Alfa-MOS Technology

AFN4192S

100V N-Channel Enhancement Mode MOSFET

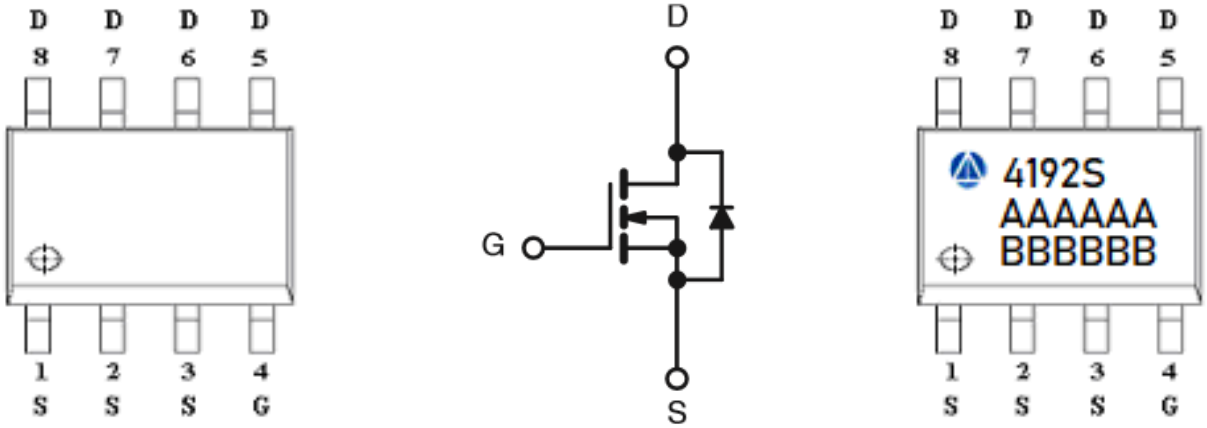
General Description

AFN4192S, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.
These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- I_D=12A,$R_{DS(ON)}$= 10mΩ@V_{GS}=10V
- I_D=10A,$R_{DS(ON)}$= 13mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- SOP-8P package design

Pin Description (SOP-8P)



Application

- Networking / Telecom / Server
- LED Lighting Applications
- Quick Charger Applications
- DC-DC Primary Side Switch

Pin Define

Pin	Symbol	Description
1~3	S	Source
4	G	Gate
5~8	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN4192SS8RG	4192S	SOP-8P	Tape & Reel	2500 EA

※ A Lot code
※ B Date code
※ AFN4192SS8RG : 13” Tape & Reel ; Pb- Free ; Halogen –Free

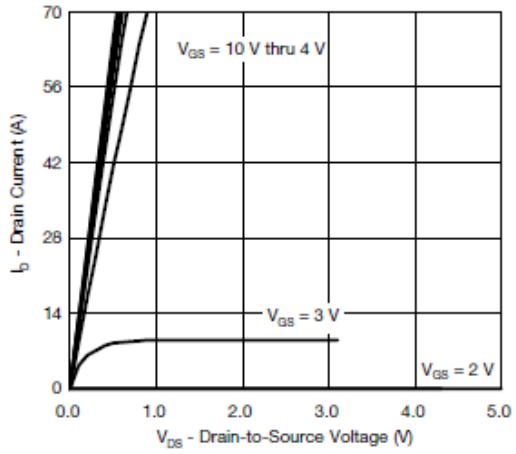
Absolute Maximum Ratings (T_A=25℃ Unless otherwise noted)

Parameter			Symbol	Typical		Unit
Drain-Source Voltage			V_{DSS}	100		V
Gate –Source Voltage			V_{GSS}	±20		V
Continuous Drain Current(T_J=150℃)	T_C=25℃	T_C=70℃	I_{DSM}	16	14	A
	T_A=25℃	T_A=70℃		12	10	
Pulsed Drain Current (t=100us)			I_{DM}	70		
Continuous Source Current(Diode Conduction)	T_C=25℃		I_S	5.0		
	T_A=25℃			2.5		
Single Pulse Avalanche Current	L=0.1mH		I_{AS}	30		
			E_{AS}	40		mJ
Power Dissipation	T_C=25℃	T_C=75℃	P_D	6	3.5	W
	T_A=25℃	T_A=75℃		3	2	
Operating Junction Temperature			T_J	150		℃
Storage Temperature Range			T_{STG}	-55/150		℃
Thermal Resistance-Junction to Ambient	t ≤ 10 s		$R_{\theta JA}$	30		℃/W
Maximum Junction-to-Case (Drain)	Steady-State		$R_{\theta JA}$	16		

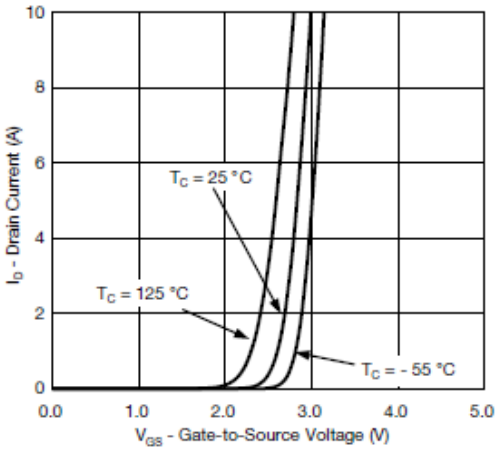
Electrical Characteristics (T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.0		2.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V			1	uA
		V_{DS}=100,V_{GS}=0V T_J=85℃			30	
On-State Drain Current	$I_{D(on)}$	V_{DS}≧5V,V_{GS}=10V	30			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=12A		7.5	10	mΩ
		V_{GS}=4.5V,I_D=10A		10	13	
Forward Transconductance	g_{FS}	V_{DS}=10,I_D=10A		54		S
Diode Forward Voltage	V_{SD}	I_S=5A,V_{GS}=0V		0.75	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=50V,V_{GS}=4.5V I_D≡10A		18	36	nC
Gate-Source Charge	Q_{gs}			6		
Gate-Drain Charge	Q_{gd}			9		
Gate Resistance	R_g	f=1MHz	0.4	1.1	2.2	Ω
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V f=1MHz		1850		pF
Output Capacitance	C_{oss}			720		
Reverse Transfer Capacitance	C_{rss}			60		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V,R_L=5Ω I_D≡10A,V_{GEN}=10V R_G=1Ω		12	24	ns
	t_r			10	20	
Turn-Off Time	$t_{d(off)}$			30	60	
	t_f			10	20	

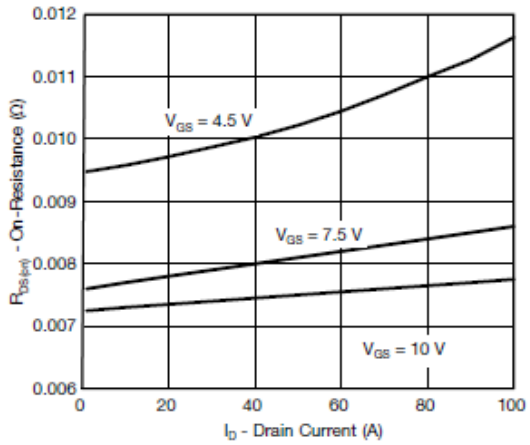
Typical Characteristics



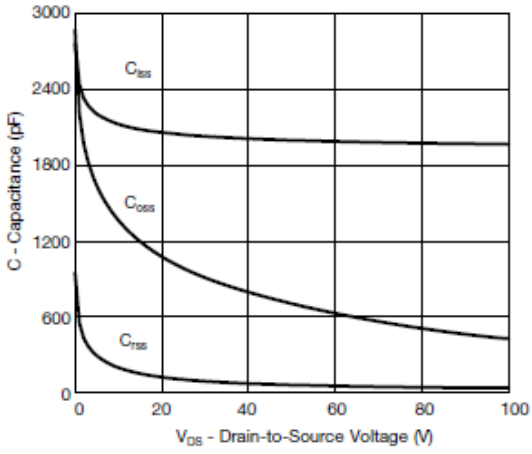
Output Characteristics



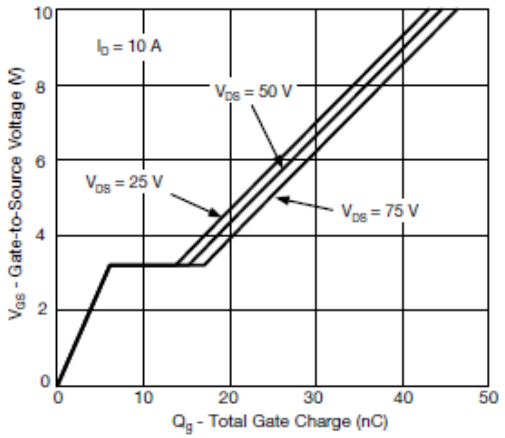
Transfer Characteristics



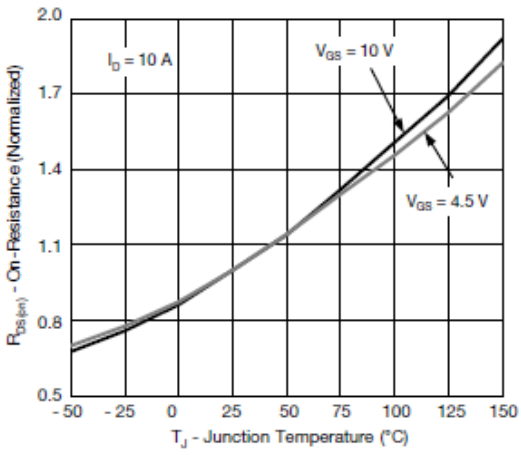
On-Resistance vs. Drain Current



Capacitance

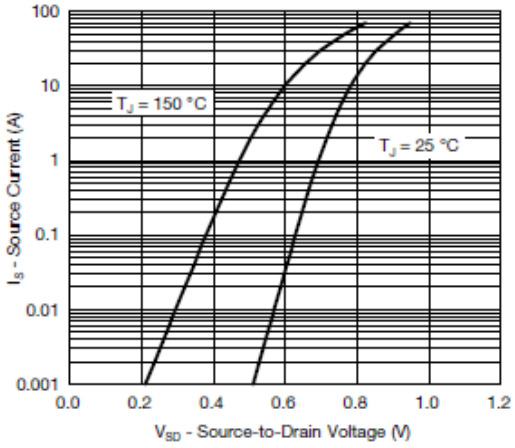


Gate Charge

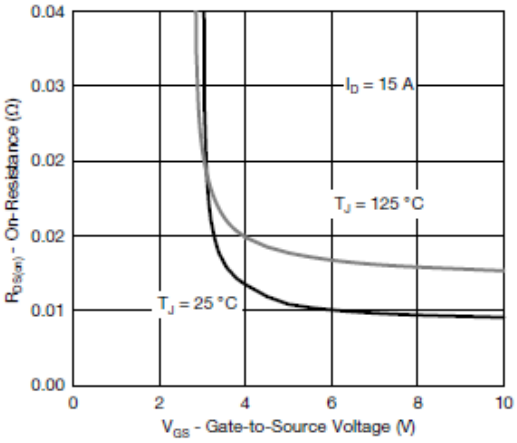


On-Resistance vs. Junction Temperature

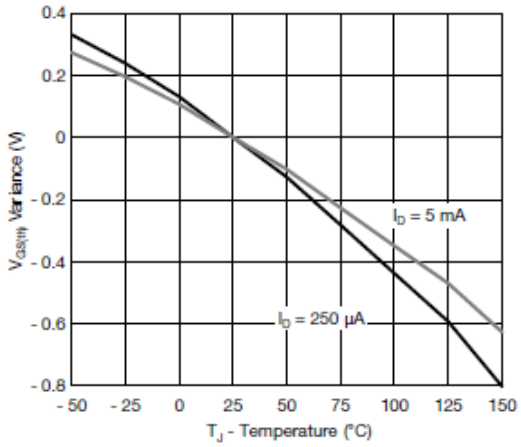
Typical Characteristics



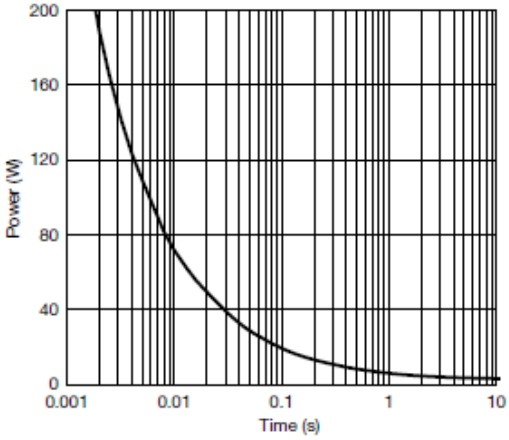
Source-Drain Diode Forward Voltage



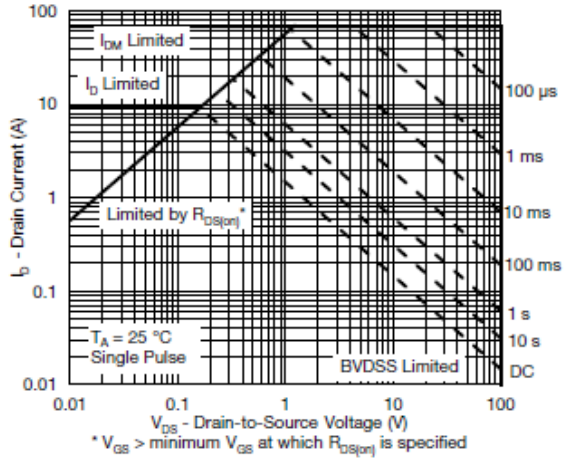
On-Resistance vs. Gate-to-Source Voltage



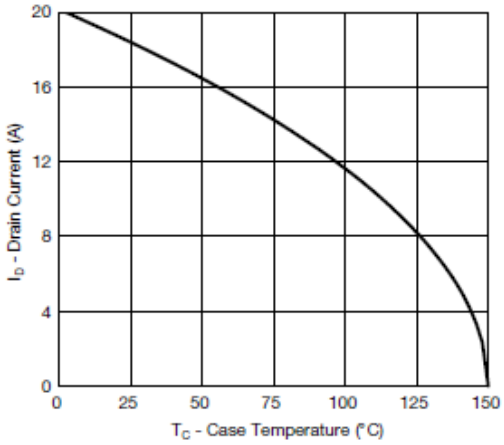
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

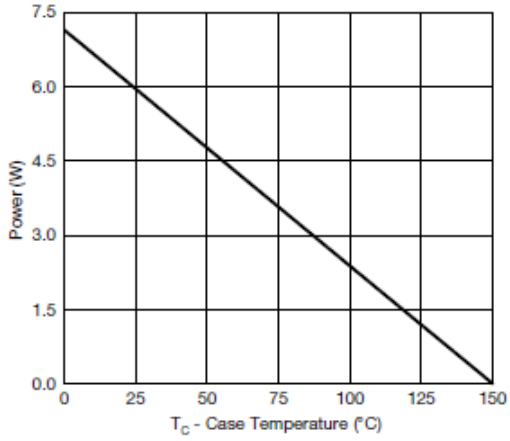


Safe Operating Area, Junction-to-Ambient

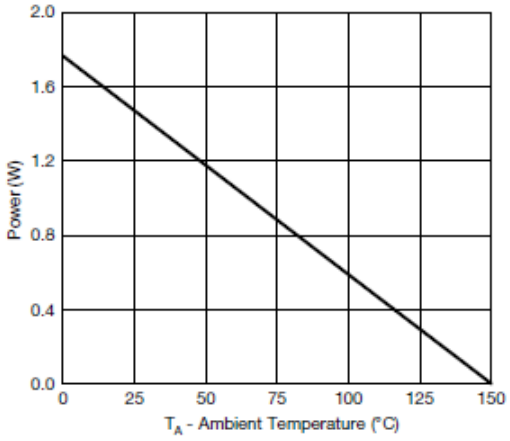


Current Derating*

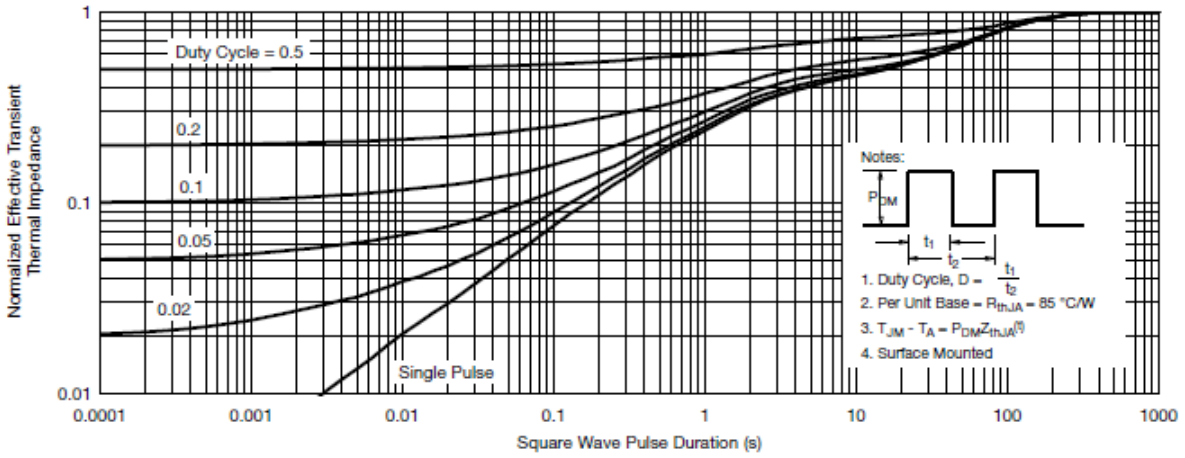
Typical Characteristics



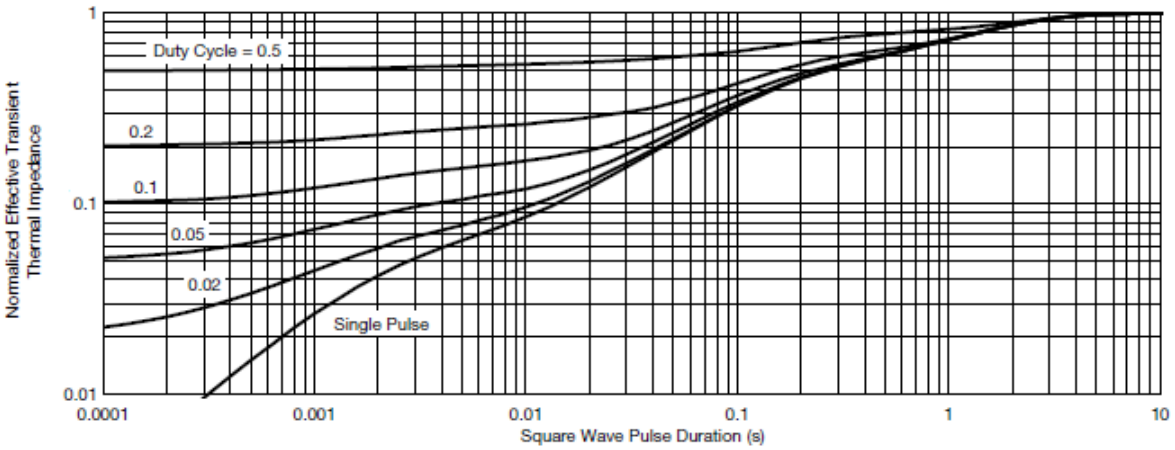
Power, Junction-to-Foot



Power, Junction-to-Ambient



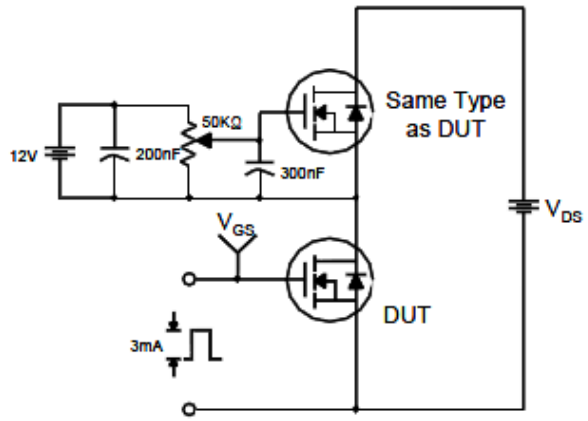
Normalized Thermal Transient Impedance, Junction-to-Ambient

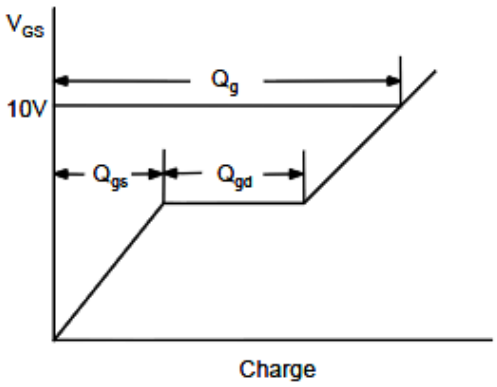


Normalized Thermal Transient Impedance, Junction-to-Foot

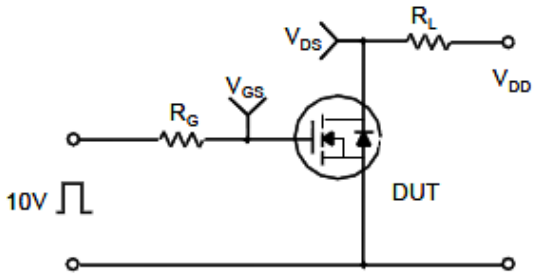
Typical Characteristics

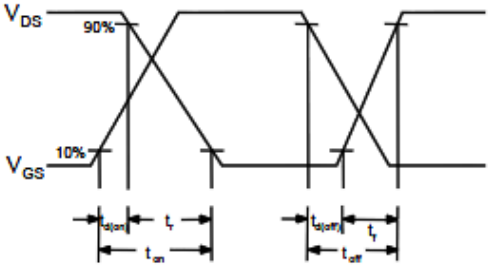
Gate Charge Test Circuit & Waveform



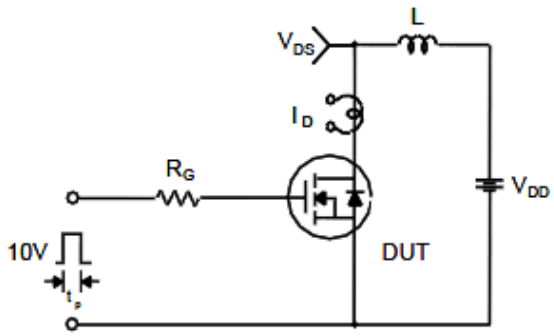


Resistive Switching Test Circuit & Waveforms

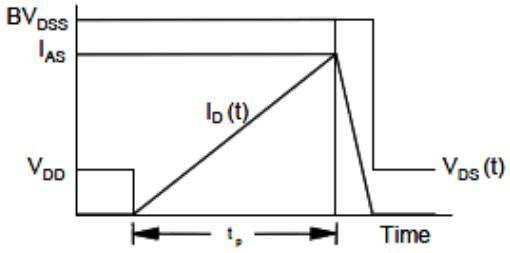




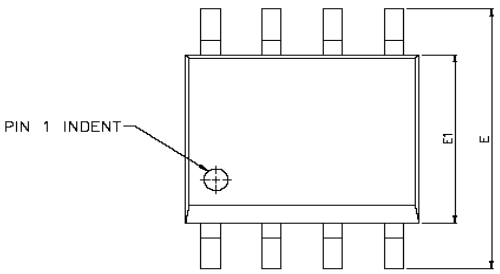
Unclamped Inductive Switching Test Circuit & Waveforms

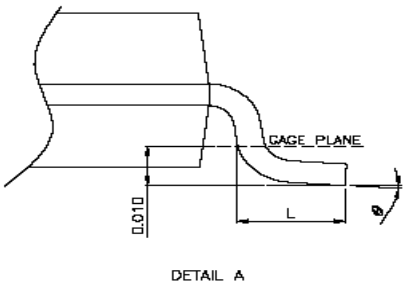


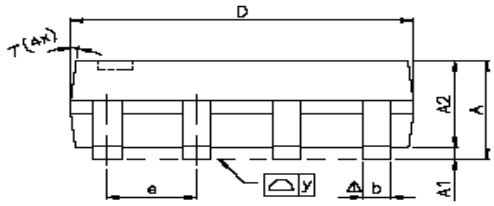
$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

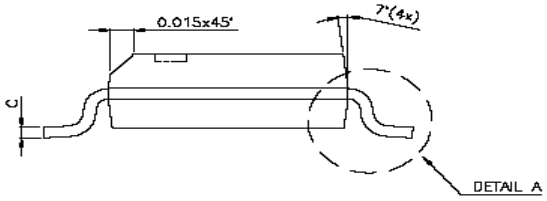


Package Information (SOP-8P)









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
② y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

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