



General Description

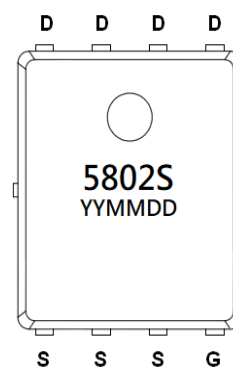
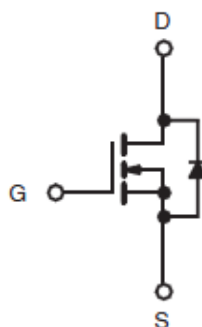
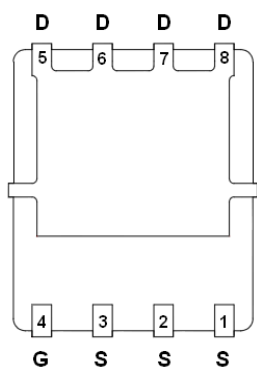
AFN5802S, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- 80V/20A, $R_{DS(ON)}=3.5m\Omega@V_{GS}=10V$
- 80V/20A, $R_{DS(ON)}=4.5m\Omega@V_{GS}=6V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- DFN5X6-8L package design

Pin Description (DFN5X6-8L)



Application

- Networking / Telecom / Server
- LED Lighting Applications
- Quick Charger Applications
- DC-DC Primary Side Switch

Pin Define

Pin	Symbol	Description
1~3	S	Source
4	G	Gate
5~8	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN5802SFN568RG	5802S	DFN5X6-8L	Tape & Reel	2500 EA

※ A Lot code

※ B Date code

※ AFN5802SFN568RG : 13" Tape & Reel ; Pb- Free ; Halogen- Free



Absolute Maximum Ratings

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	80	V
Gate –Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J=150^\circ\text{C}$)	$T_C=25^\circ\text{C}$	110	A
	$T_C=70^\circ\text{C}$	110	
Pulsed Drain Current ($t=100\mu\text{s}$)	$T_A=25^\circ\text{C}$	36	
	$T_A=70^\circ\text{C}$	30	
Continuous Source Current(Diode Conduction)	I_S	90	mJ
Single Pulse Avalanche Current	$L=0.1\text{mH}$	45	
Power Dissipation	$T_C=25^\circ\text{C}$	105	W
	$T_C=75^\circ\text{C}$	65	
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient	$t \leq 10\text{ s}$	20	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	Steady-State	1.2	

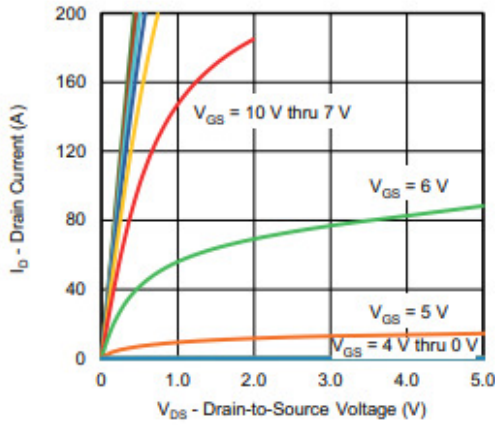
Electrical Characteristics

($T_A=25^\circ\text{C}$ Unless otherwise noted)

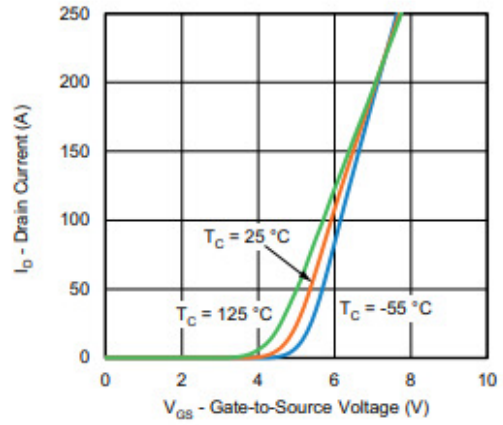
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	80			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.0	2.8	4.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=64\text{V}, V_{GS}=0\text{V}$			1	uA
		$V_{DS}=64\text{V}, V_{GS}=0\text{V}$ $T_J=85^\circ\text{C}$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5\text{V}, V_{GS}=10\text{V}$	30			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=20\text{A}$		2.3	3.5	m Ω
		$V_{GS}=6.0\text{V}, I_D=20\text{A}$		3.1	4.5	
Forward Transconductance	g_{FS}	$V_{DS}=15\text{V}, I_D=20\text{A}$		50		S
Diode Forward Voltage	V_{SD}	$I_S=5\text{A}, V_{GS}=0\text{V}$		0.75	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=40\text{V}, V_{GS}=7.5\text{V}$ $I_D=20\text{A}$		40	80	nC
Gate-Source Charge	Q_{gs}			16		
Gate-Drain Charge	Q_{gd}			8		
Gate Resistance	R_g	$f=1\text{MHz}$	0.4	1.4	2.4	Ω
Input Capacitance	C_{iss}	$V_{DS}=40\text{V}, V_{GS}=0\text{V}$ $f=1\text{MHz}$		4150		pF
Output Capacitance	C_{oss}			900		
Reverse Transfer Capacitance	C_{rss}			20		
Turn-On Time	$t_{d(on)}$	$V_{DD}=40\text{V}, R_L=2.0\Omega$ $I_D=20\text{A}, V_{GEN}=10\text{V}$ $R_G=1\Omega$		16	32	ns
	t_r			12	24	
Turn-Off Time	$t_{d(off)}$			26	52	
	t_f			12	24	



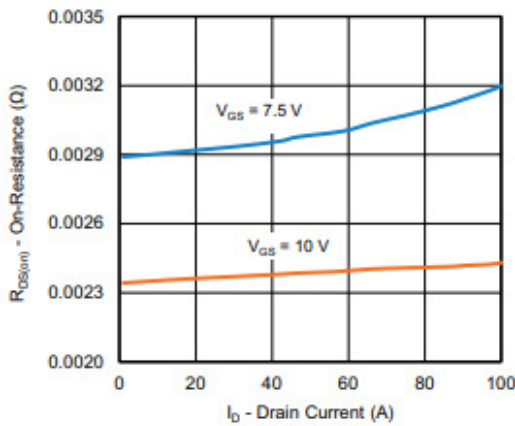
Typical Characteristics



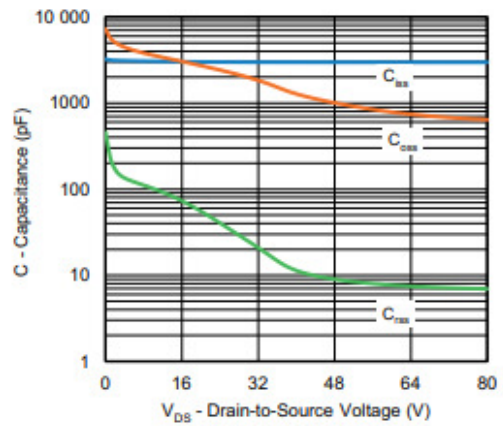
Output Characteristics



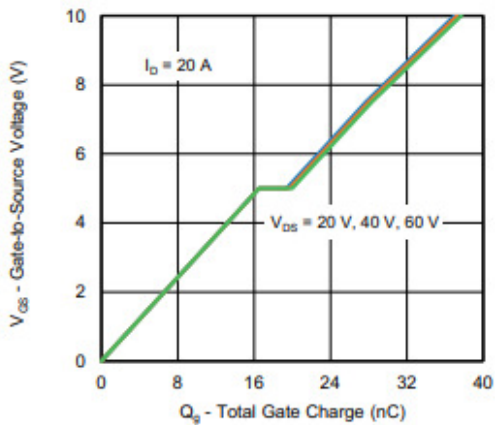
Transfer Characteristics



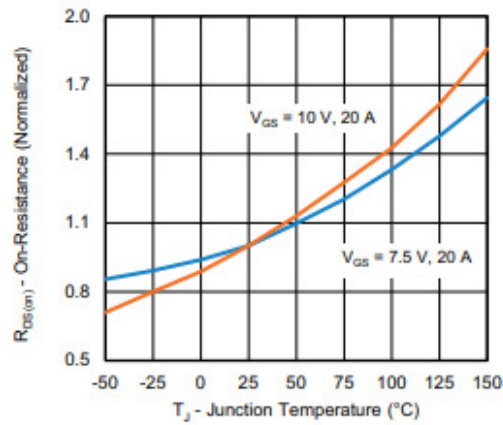
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



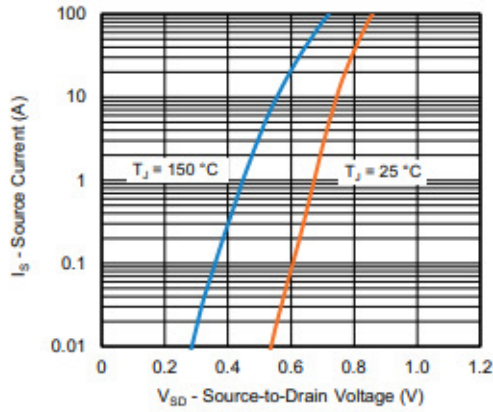
Gate Charge



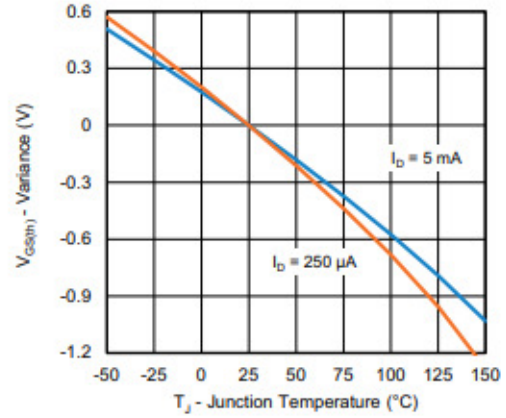
On-Resistance vs. Junction Temperature



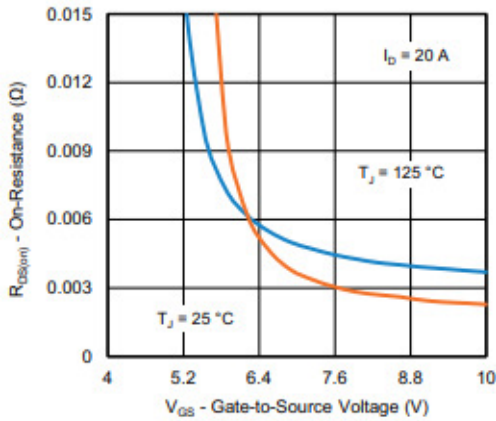
Typical Characteristics



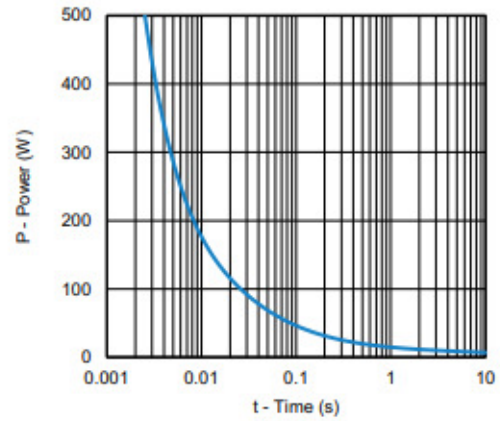
Source-Drain Diode Forward Voltage



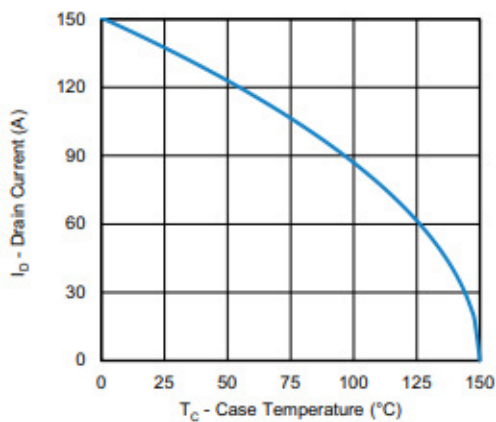
Threshold Voltage



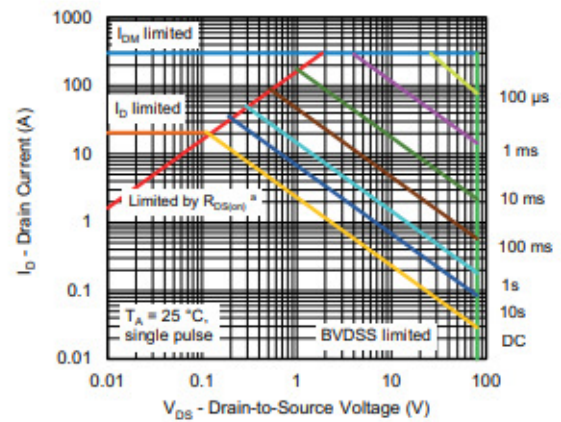
On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



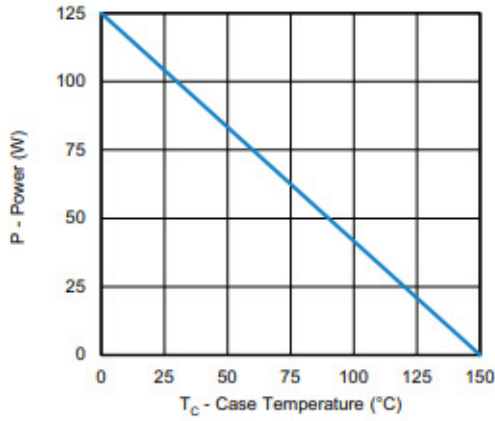
Current Derating ^a



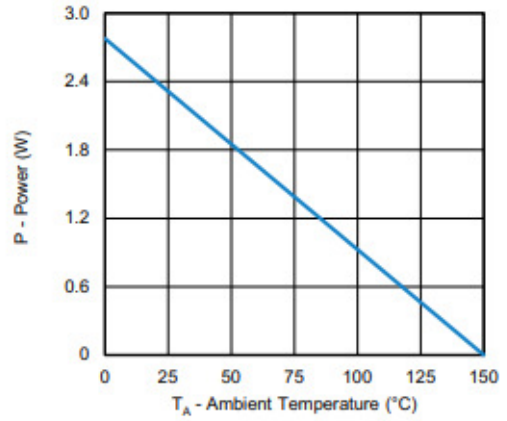
Safe Operating Area, Junction-to-Ambient



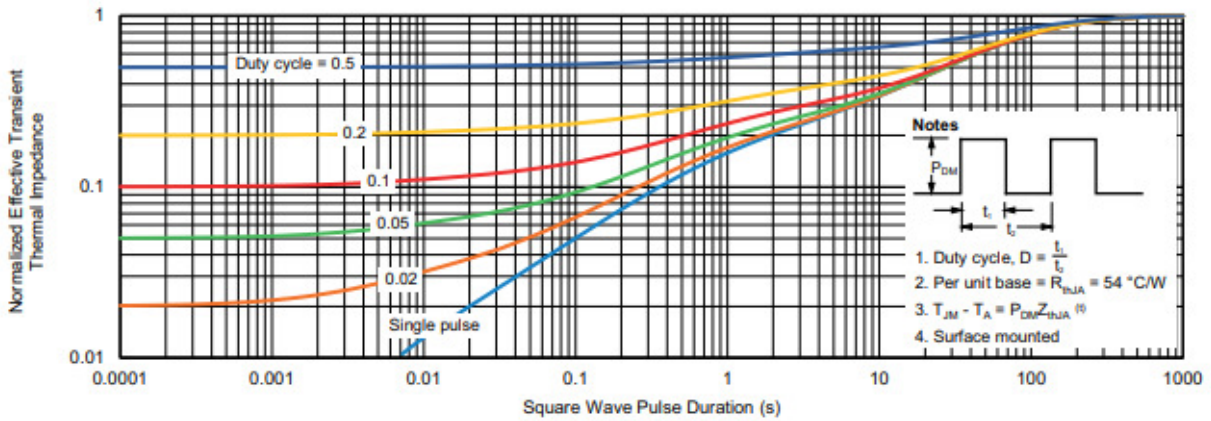
Typical Characteristics



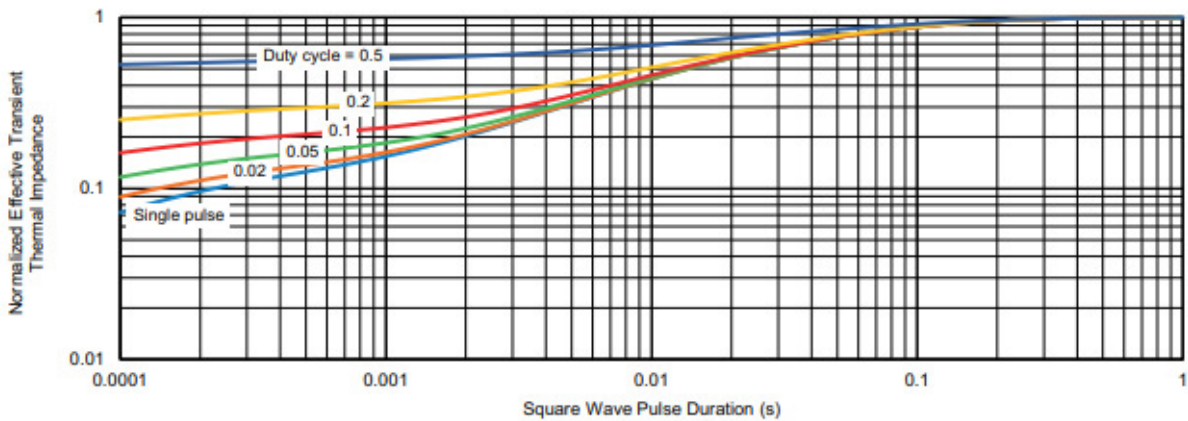
Power, Junction-to-Case



Power, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

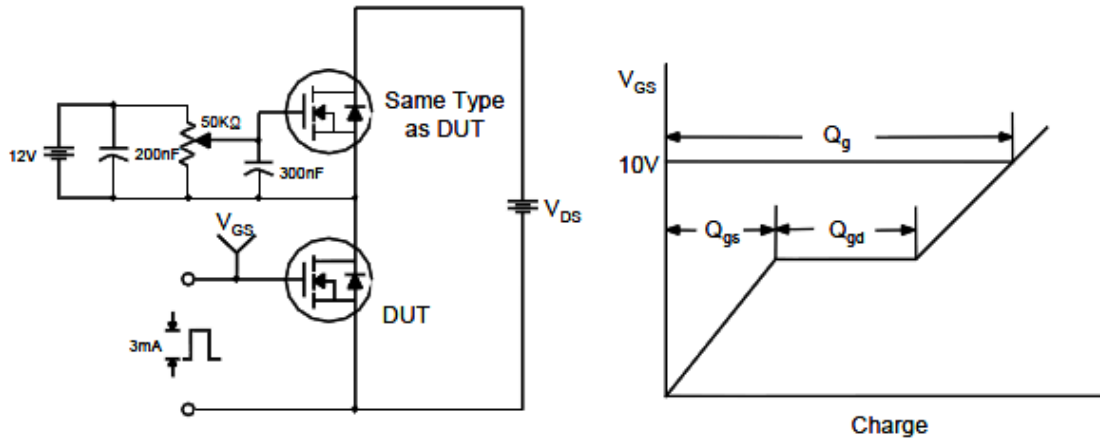


Normalized Thermal Transient Impedance, Junction-to-Case

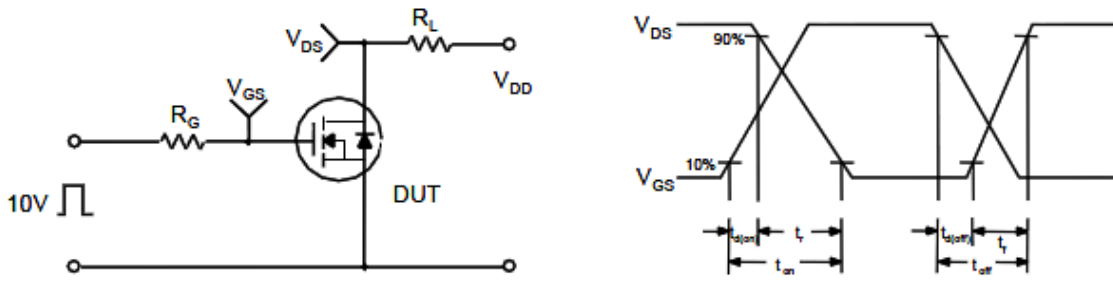


Typical Characteristics

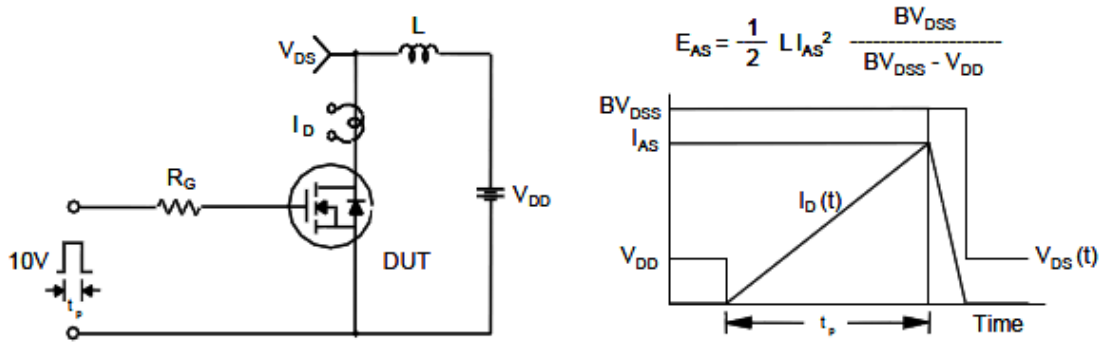
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

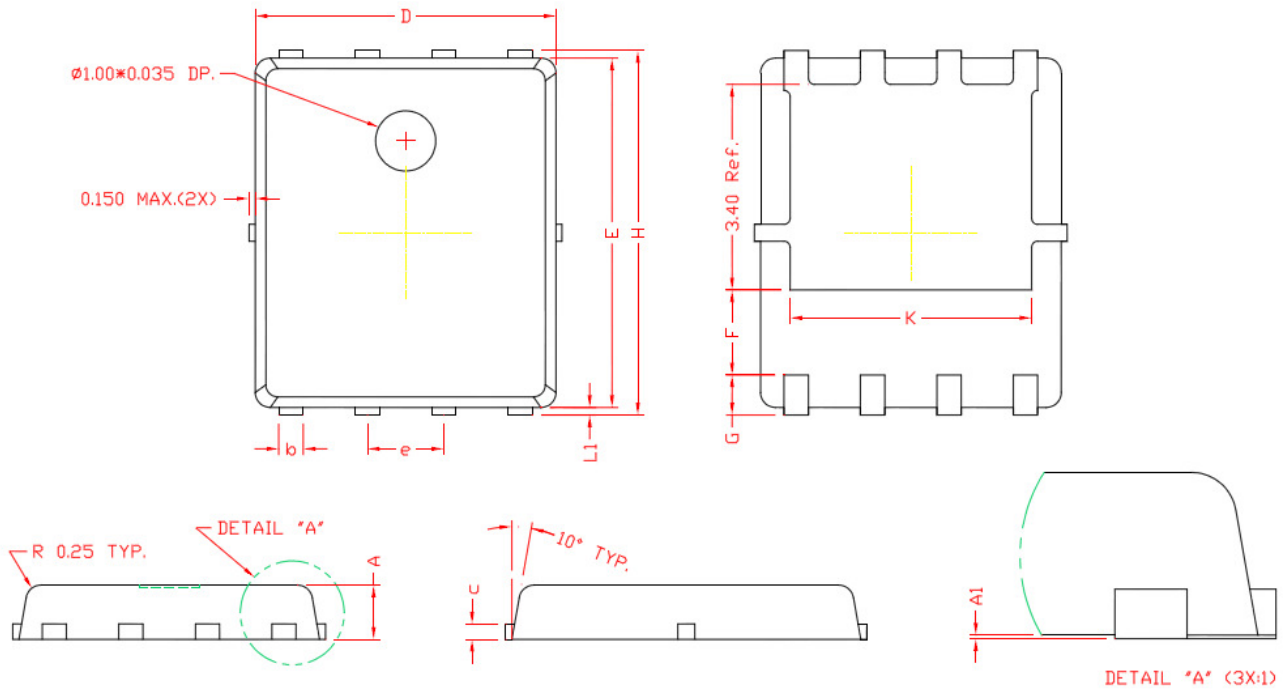


Unclamped Inductive Switching Test Circuit & Waveforms





Package Information (DFN5X6-8L)



DIMENSIONS

REF.	Millimeters		REF.	Millimeters	
	Min.	Max.		Min.	Max.
A	0.80	1.00	E	5.70	5.90
A1	0.00	0.05	e	1.27 BSC.	
b	0.35	0.49	H	5.95	6.20
c	0.254 Ref.		L1	0.10	0.18
D	4.90	5.10	G	0.60 Ref.	
F	1.40 Ref.		K	4.00 Ref.	

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