



General Description

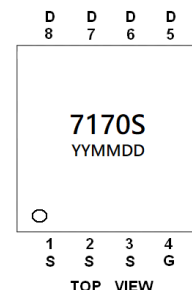
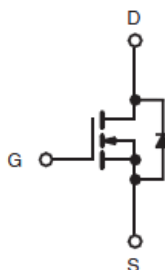
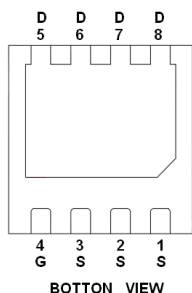
AFN7170S, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, such as smart phone and notebook computer and other battery powered circuits, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- 100V/9A, $R_{DS(ON)} = 37m\Omega @ V_{GS} = 10V$
- 100V/8A, $R_{DS(ON)} = 40m\Omega @ V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- DFN3X3-8L package design

Pin Description (DFN3X3-8L)



Application

- Primary Side Switch
- Synchronous Rectification
- DC/DC Converters & DC/AC Inverters
- Boost Converters

Pin Define

Pin	Symbol	Description
1~3	S	Source
4	G	Gate
5~8	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN7170SFN338RG	7170S	DFN3X3-8L	Tape & Reel	5000 EA

※ YY year code

※ MM month code

※ DD date code

※ AFN7170SFN338RG : 13" Tape & Reel ; Pb- Free ; Halogen -Free



Absolute Maximum Ratings

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate –Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J=150^\circ\text{C}$)	I_D	$T_A=25^\circ\text{C}$	9
		$T_A=70^\circ\text{C}$	8
Pulsed Drain Current	I_{DM}	20	A
Continuous Source Current(Diode Conduction)	I_S	1.5	A
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	2.8
		$T_A=70^\circ\text{C}$	1.8
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

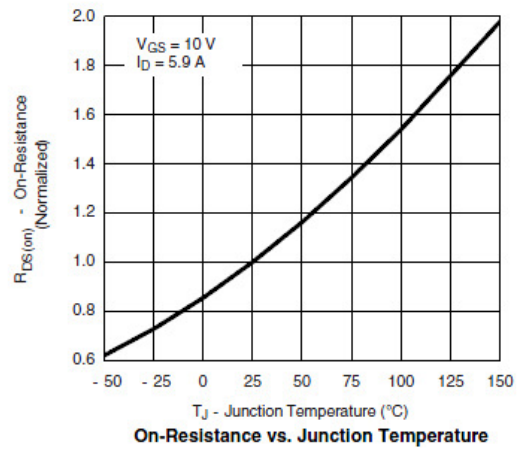
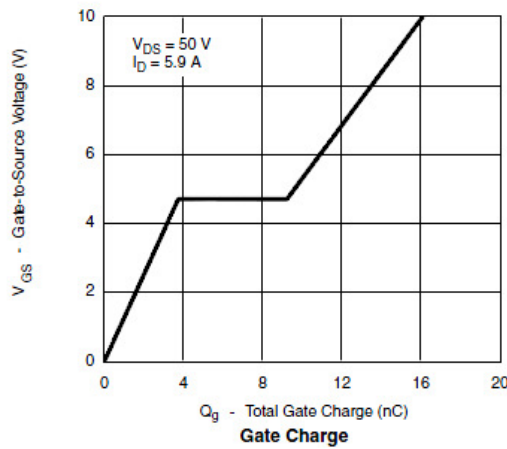
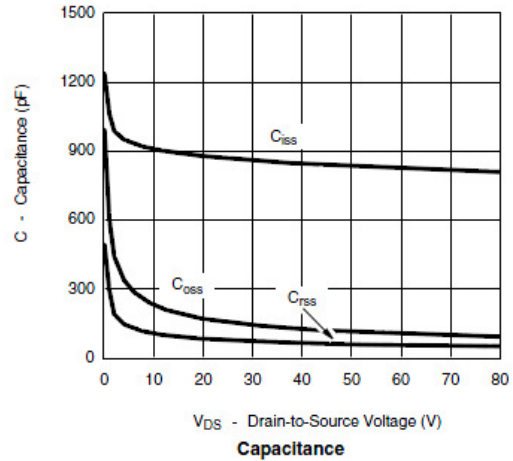
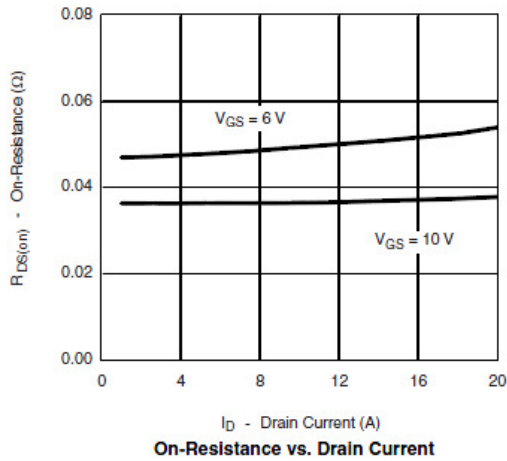
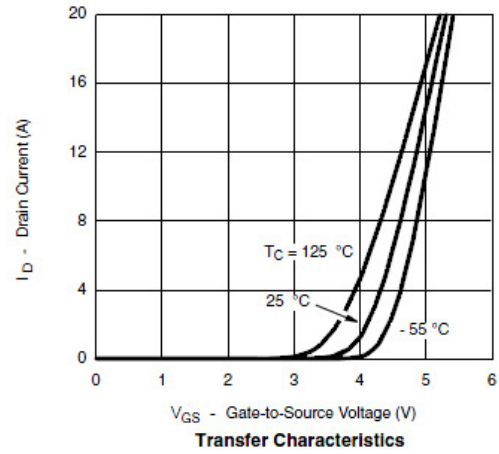
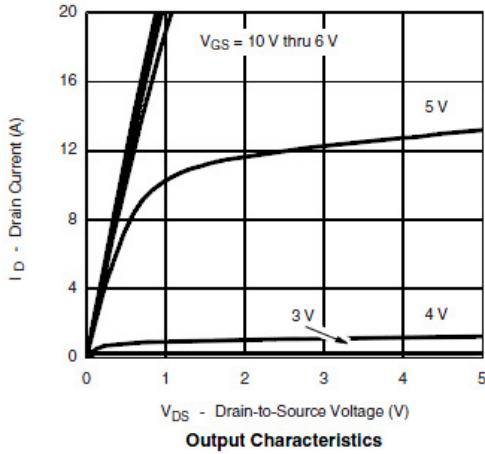
Electrical Characteristics

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu\text{A}$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0		2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$			1	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=85^\circ\text{C}$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=4.5V$	20			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=9A$		27	37	m Ω
		$V_{GS}=4.5V, I_D=8A$		30	40	
Forward Transconductance	g_{FS}	$V_{DS}=15V, I_D=6A$		14		S
Diode Forward Voltage	V_{SD}	$I_S=2A, V_{GS}=0V$		0.8	1.3	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=50V, V_{GS}=10V$ $I_D=6A$		16	24	nC
Gate-Source Charge	Q_{gs}		4.0			
Gate-Drain Charge	Q_{gd}		6.0			
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V$ $f=1\text{MHz}$		850		pF
Output Capacitance	C_{oss}		90			
Reverse Transfer Capacitance	C_{rss}		40			
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, R_L=50\Omega$ $I_D=1.0A, V_{GEN}=10V$ $R_G=6\Omega$		15	25	ns
	t_r			15	25	
Turn-Off Time	$t_{d(off)}$			35	55	
	t_f			20	35	

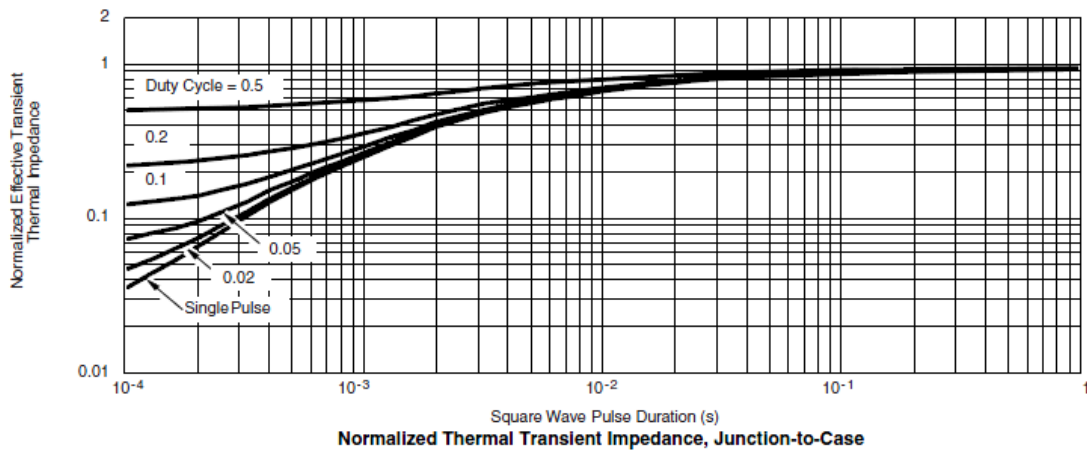
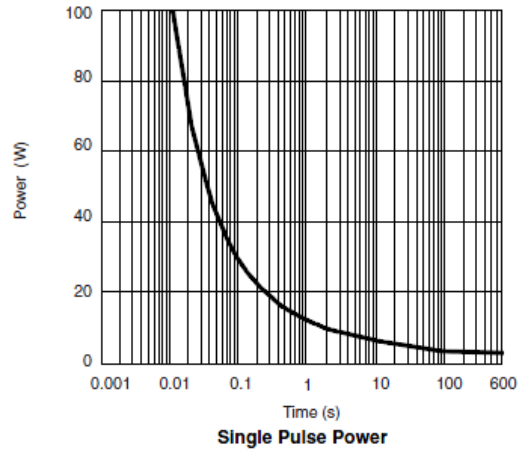
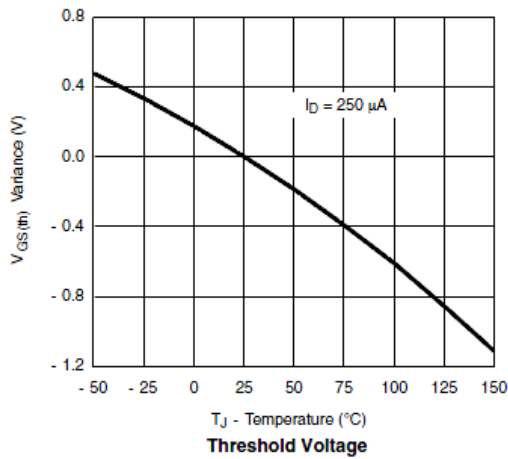
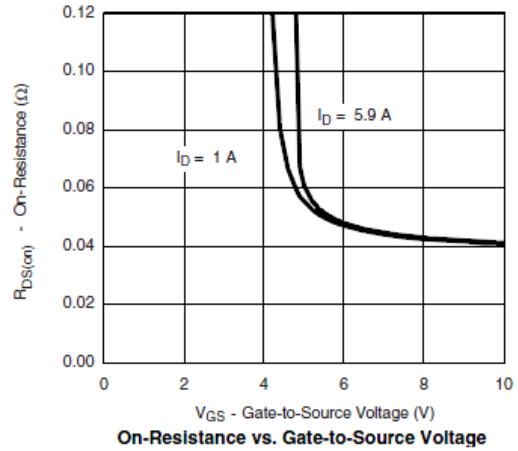
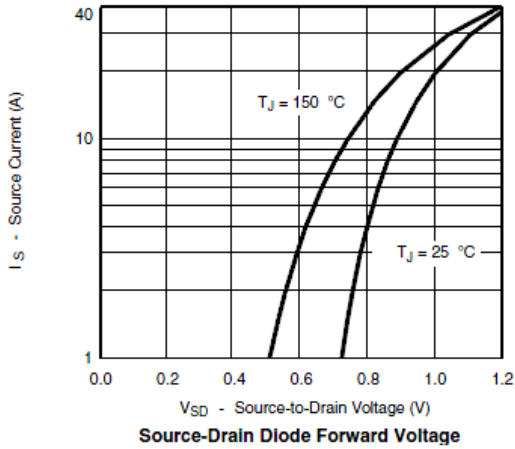


Typical Characteristics





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Typical Characteristics

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

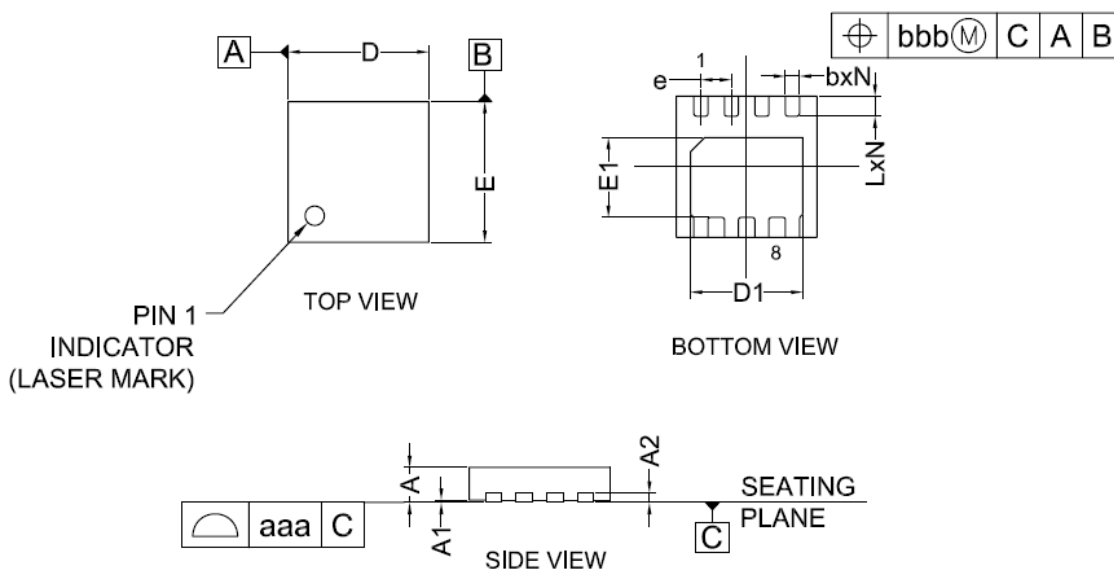


Unclamped Inductive Switching Test Circuit & Waveforms





Package Information (DFN3X3-8L)



SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.203		
b	0.25	0.30	0.35
D	2.90	3.00	3.10
D1	2.35	2.40	2.45
E	2.90	3.00	3.10
E1	1.65	1.70	1.75
e	0.65BSC		
L	0.37	0.42	0.47
N	8		
aaa	0.08		
bbb	0.10		

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

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