



## General Description

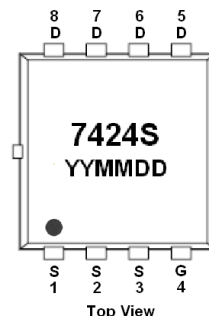
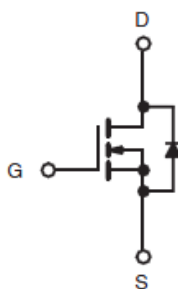
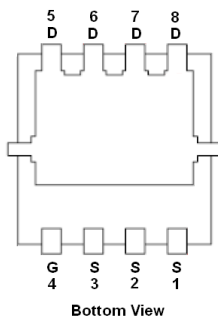
AFN7424S, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent  $R_{DS(ON)}$ , low gate charge.

These devices are particularly suited for low voltage power management, such as smart phone and notebook computer and other battery powered circuits, and low in-line power loss are needed in commercial industrial surface mount applications.

## Features

- $I_D=20A, R_{DS(ON)}=4.5m\Omega@V_{GS}=10V$
- $I_D=15A, R_{DS(ON)}=6.5m\Omega@V_{GS}=4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- DFN3.3X3.3-8L package design

## Pin Description ( DFN3.3X3.3-8L )



## Application

- DC-DC Converter
- POL

## Pin Define

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

## Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN7424SFN308RG	7424S	DFN3.3X3.3-8L	Tape & Reel	5000 EA

※ YY year code

※ MM month code

※ DD date code

※ AFN7424SFN308RG : 13" Tape & Reel ; Pb- Free ; Halogen -Free



**Absolute Maximum Ratings**

(T<sub>A</sub>=25°C Unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	30	V
Gate –Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>A</sub> =25°C	20
		T <sub>A</sub> =70°C	15
Pulsed Drain Current	I <sub>DM</sub>	70	A
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	40	A
Power Dissipation	P <sub>D</sub>	T <sub>C</sub> =25°C	28
		T <sub>C</sub> =70°C	15
		T <sub>A</sub> =25°C	3.1
		T <sub>A</sub> =70°C	2.0
Operating Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance Junction-to-Case (Drain)	R <sub>θJC</sub>	5	°C/W
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	40	

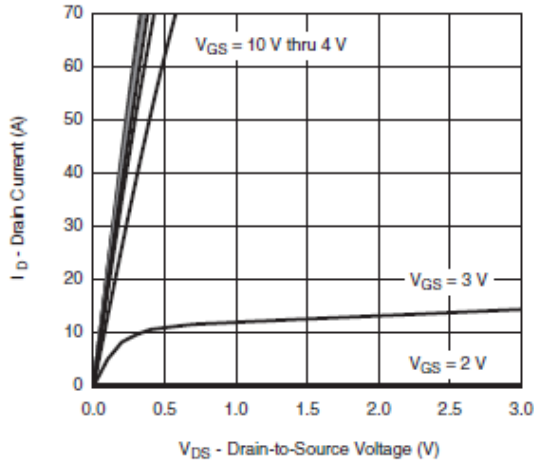
**Electrical Characteristics**

(T<sub>A</sub>=25°C Unless otherwise noted)

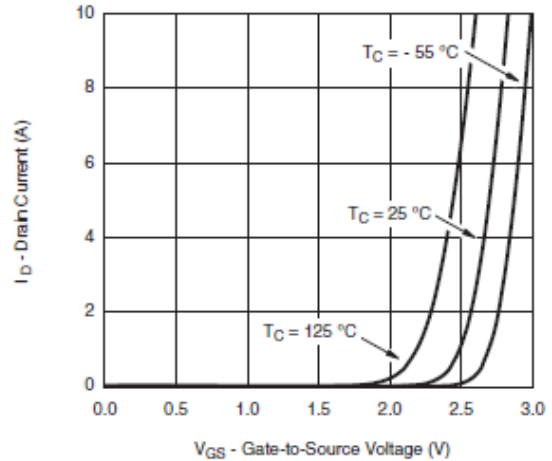
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1.0		2.0	
Gate Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V			1	uA
		V <sub>DS</sub> =24V, V <sub>GS</sub> =0V T <sub>J</sub> =85°C			10	
On-State Drain Current	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5V, V <sub>GS</sub> =10V	50			A
Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		3.6	4.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A		5.5	6.5	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =20 A		80		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =10A, V <sub>GS</sub> =0V		0.8	1.3	V
<b>Dynamic</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =4.5V I <sub>D</sub> ≡20A		15	25	nC
Gate-Source Charge	Q <sub>gs</sub>			6		
Gate-Drain Charge	Q <sub>gd</sub>			5		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V f=1MHz		1800		pF
Output Capacitance	C <sub>oss</sub>			350		
Reverse Transfer Capacitance	C <sub>rss</sub>			150		
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> =15V, R <sub>L</sub> =1.5Ω I <sub>D</sub> ≡10A, V <sub>GEN</sub> =10V		12	20	ns
	t <sub>r</sub>			10	20	
Turn-Off Time	t <sub>d(off)</sub>	R <sub>G</sub> =1.0Ω		25	45	
	t <sub>f</sub>			10	20	



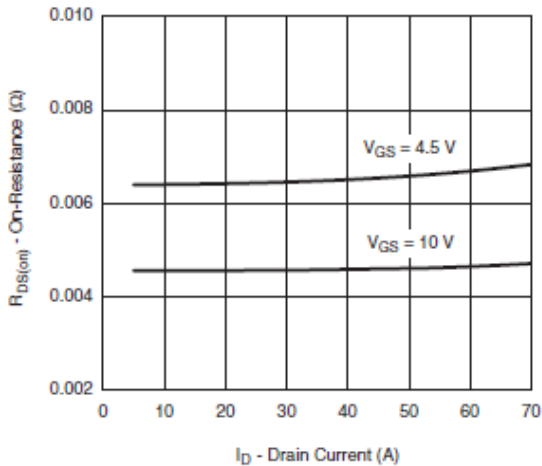
## Typical Characteristics



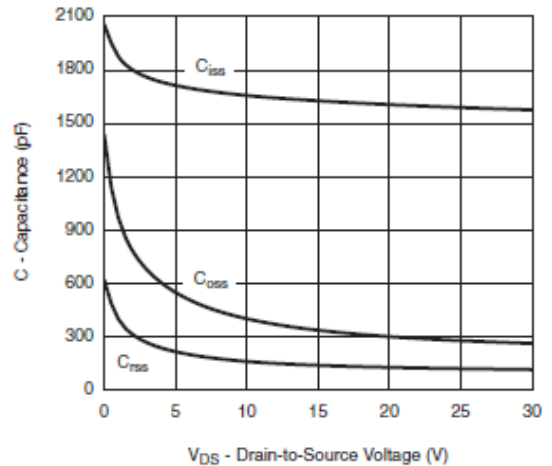
Output Characteristics



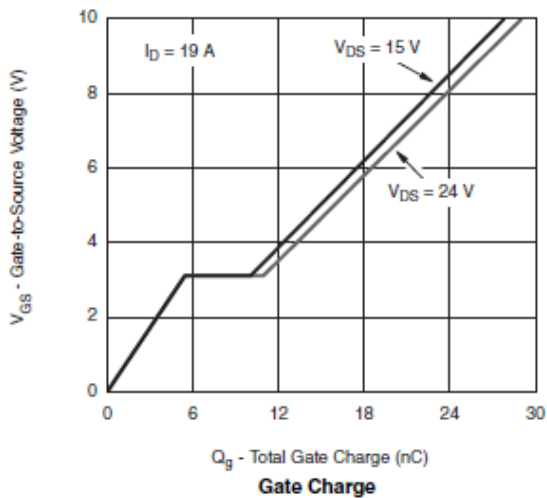
Transfer Characteristics



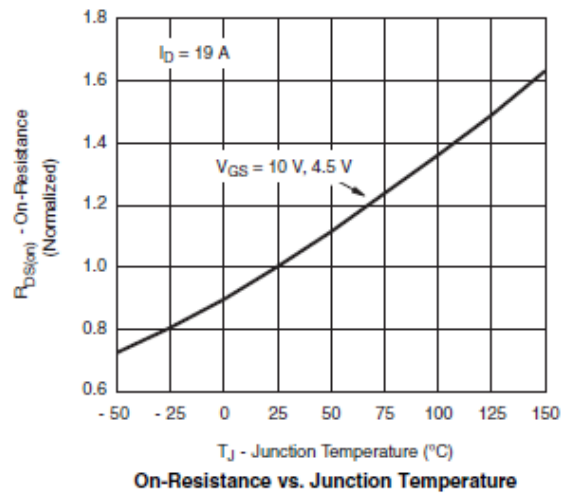
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



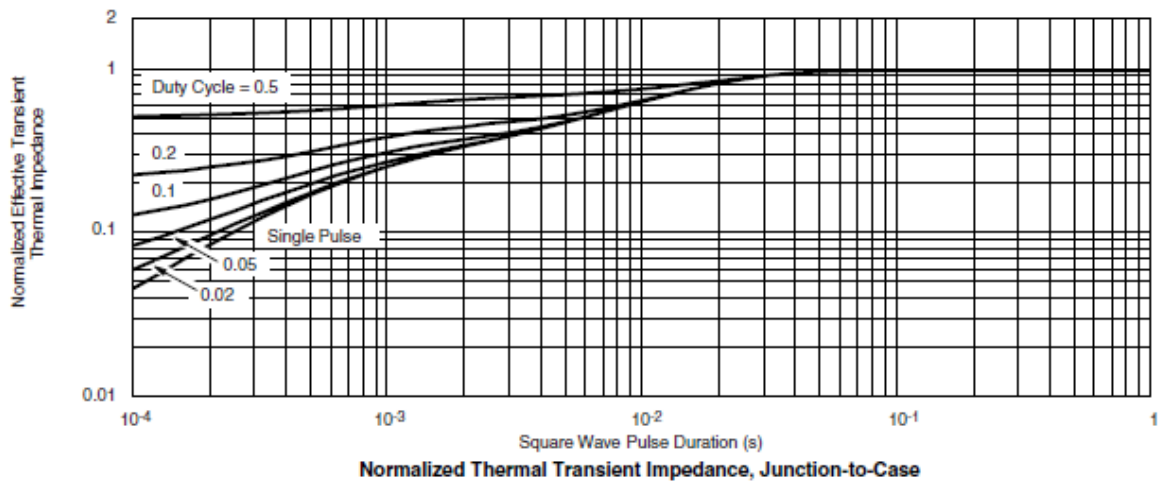
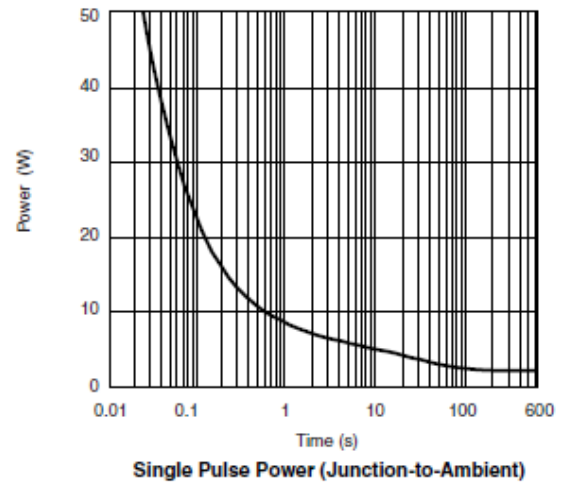
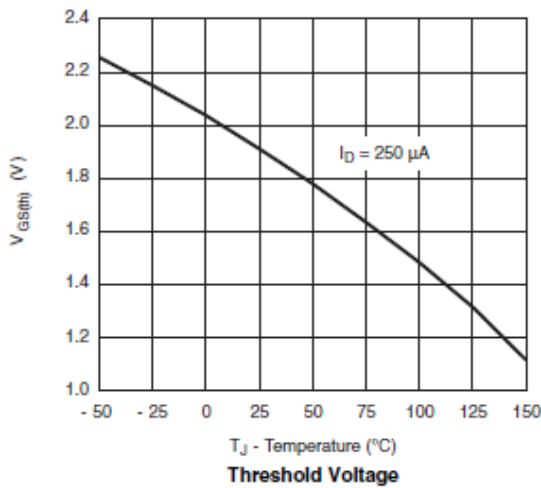
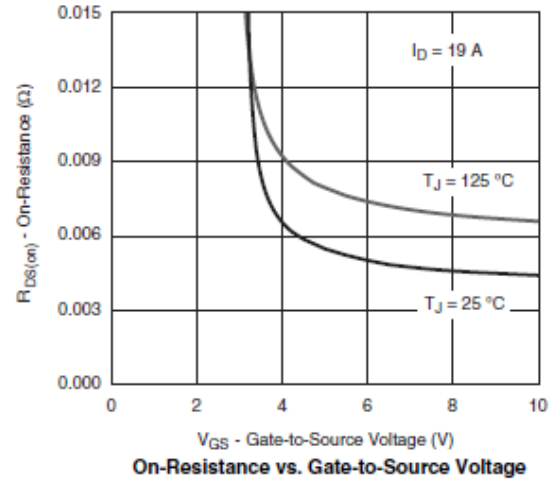
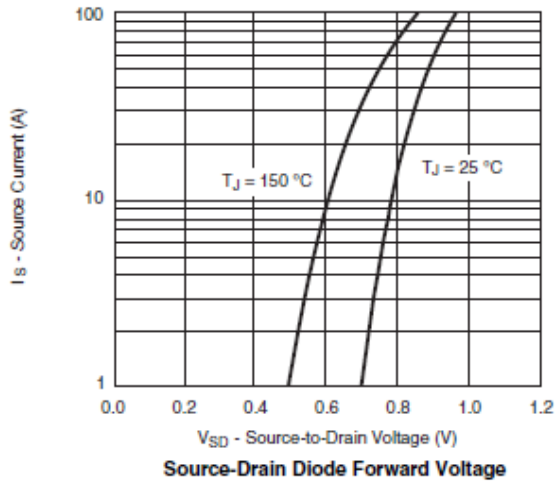
Gate Charge



On-Resistance vs. Junction Temperature



## Typical Characteristics





**Typical Characteristics**

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

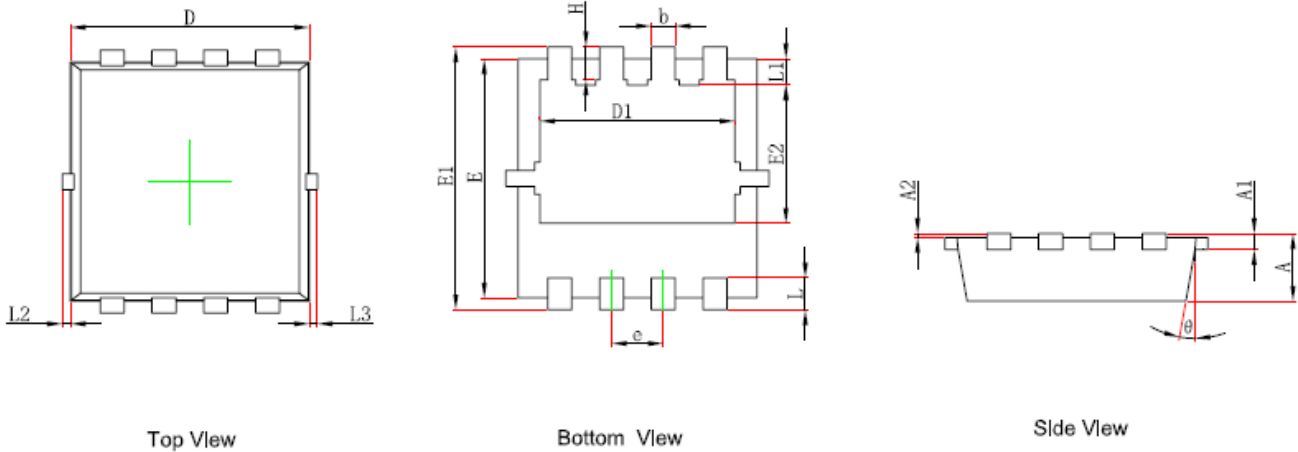


Unclamped Inductive Switching Test Circuit & Waveforms





**Package Information ( DFN3.3X3.3-8L )**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

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 2F, No.80, Sec.1, Cheng Kung Rd., Nan Kang Dist., Taipei City 115, Taiwan (R.O.C.)  
 Tel : 886 2) 2651 3928  
 Fax : 886 2) 2786 8483  
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