



General Description

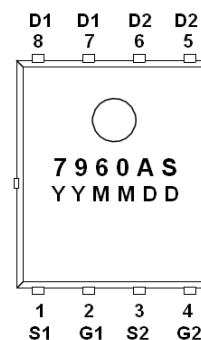
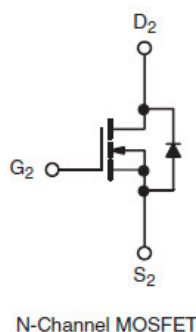
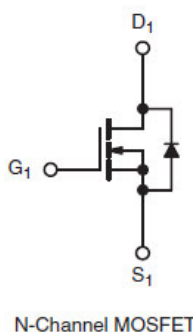
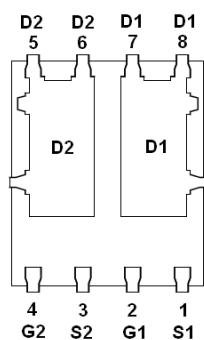
AFN7960AS, Dual N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- 60V/12A, $R_{DS(ON)} = 20m\Omega @ V_{GS} = 10V$
- 60V/10A, $R_{DS(ON)} = 24m\Omega @ V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- DFN 5X6-8L package design

Pin Description (DFN5X6-8L)



Application

- Motor and Load Control
- Power Management in White LED System
- LCD TV Inverter & AD/DC Inverter Systems.

Pin Define

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	S2	Source 2
4	G2	Gate 2
5	D2	Drain 2
6	D2	Drain 2
7	D1	Drain 1
8	D1	Drain 1

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN7960ASFN568RG	7960AS	DFN 5X6-8L	Tape & Reel	2500 EA

※ 7960AS : Parts Code

※ YYMMDD : Date Code

※ AFN7960ASFN568RG : 13" Tape & Reel ; Pb- Free ; Halogen- Free



Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate –Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J=150^\circ\text{C}$)	I_D	$T_A=25^\circ\text{C}$	12
		$T_A=85^\circ\text{C}$	10
Pulsed Drain Current	I_{DM}	40	A
Continuous Source Current(Diode Conduction)	I_S	2.9	A
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	3.5
		$T_A=70^\circ\text{C}$	2.2
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

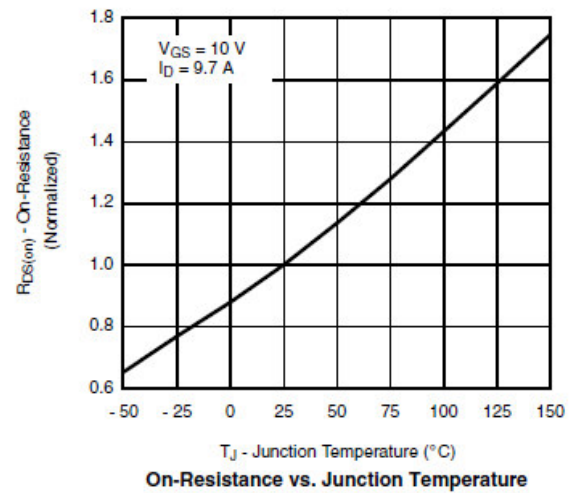
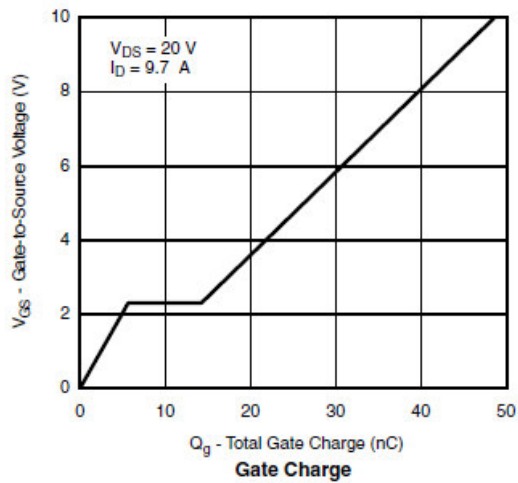
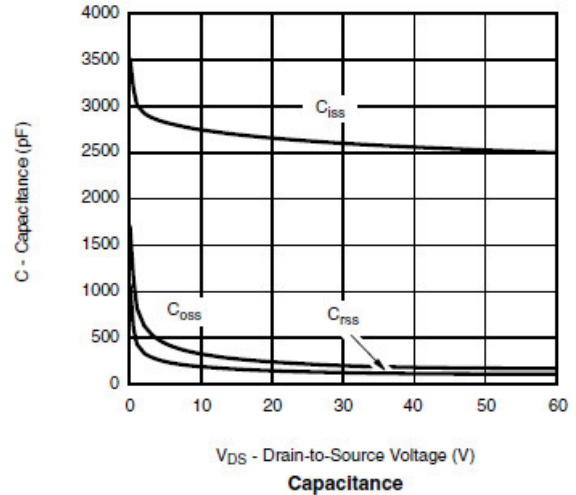
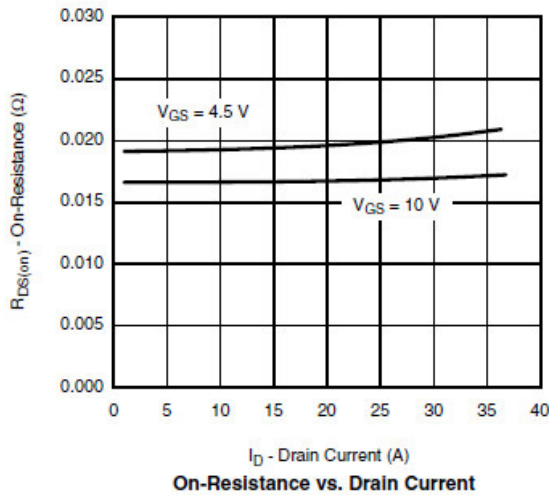
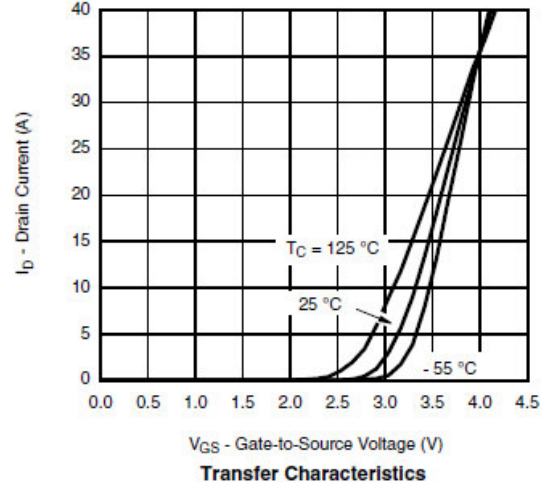
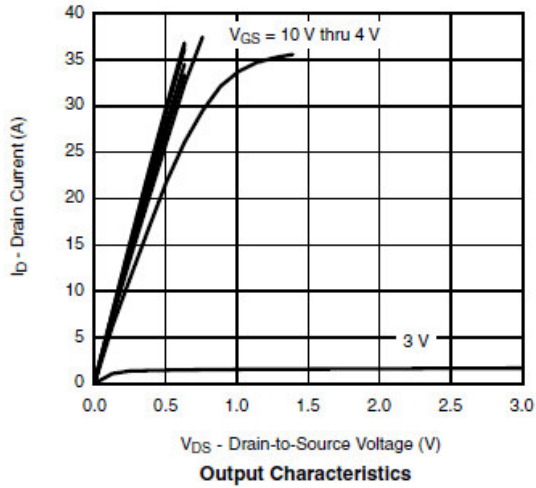
Electrical Characteristics

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=48V, V_{GS}=0V$			1	uA
		$V_{DS}=48V, V_{GS}=0V$ $T_J=85^\circ\text{C}$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$	30			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=12A$		17	20	m Ω
		$V_{GS}=4.5V, I_D=10A$		19	24	
Forward Transconductance	g_{FS}	$V_{DS}=15V, I_D=5.3A$		24		S
Diode Forward Voltage	V_{SD}	$I_S=2.0A, V_{GS}=0V$		0.85	1.3	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=30V, V_{GS}=10V$ $I_D \equiv 9.7A$		50	75	nC
Gate-Source Charge	Q_{gs}			6		
Gate-Drain Charge	Q_{gd}			9		
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V$ $f=1\text{MHz}$		3200		pF
Output Capacitance	C_{oss}			300		
Reverse Transfer Capacitance	C_{rss}			250		
Turn-On Time	$t_{d(on)}$	$V_{DD}=30V, R_L=30\Omega$ $I_D \equiv 1A, V_{GEN}=10V$ $R_G=6\Omega$		12	20	ns
	t_r			12	20	
Turn-Off Time	$t_{d(off)}$			60	90	
	t_f			20	30	

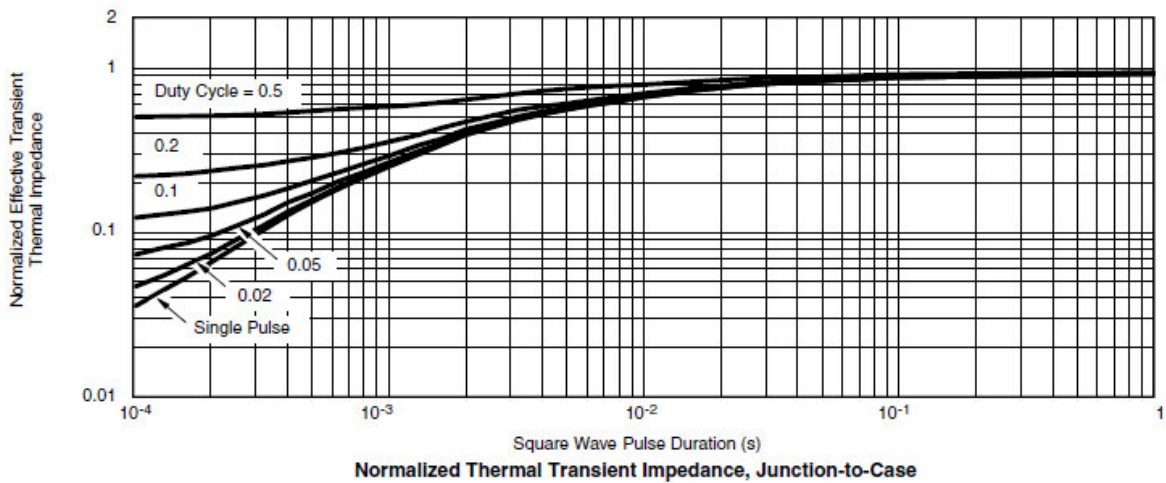
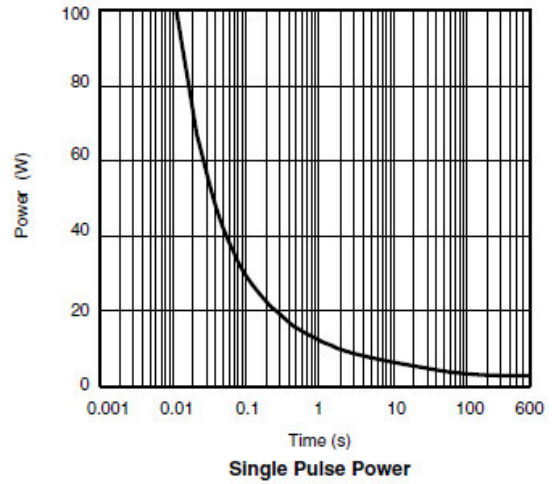
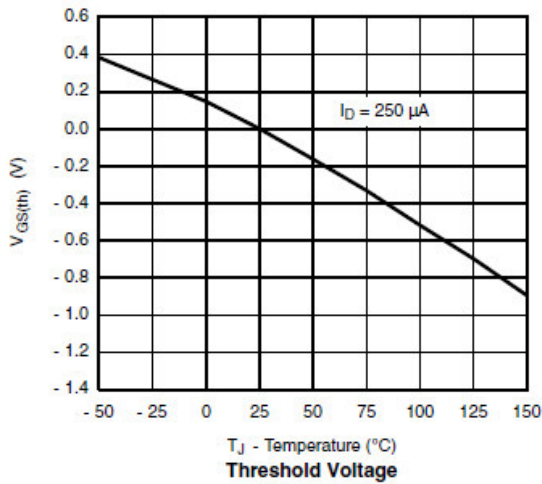
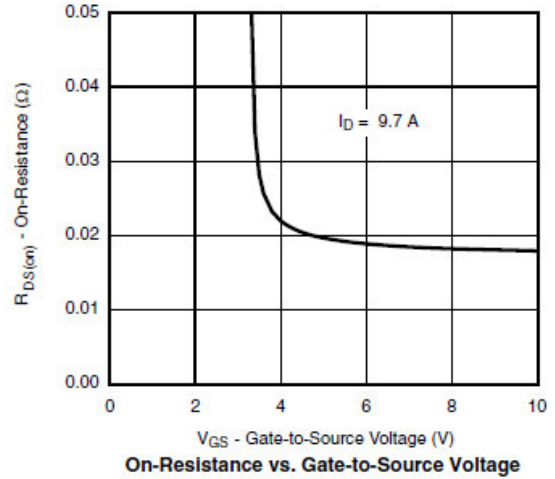
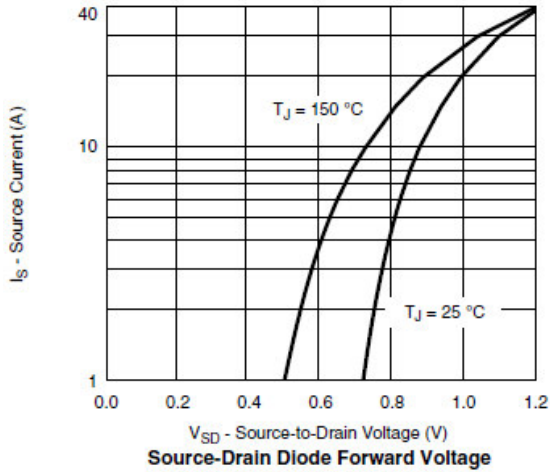


Typical Characteristics





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Typical Characteristics

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

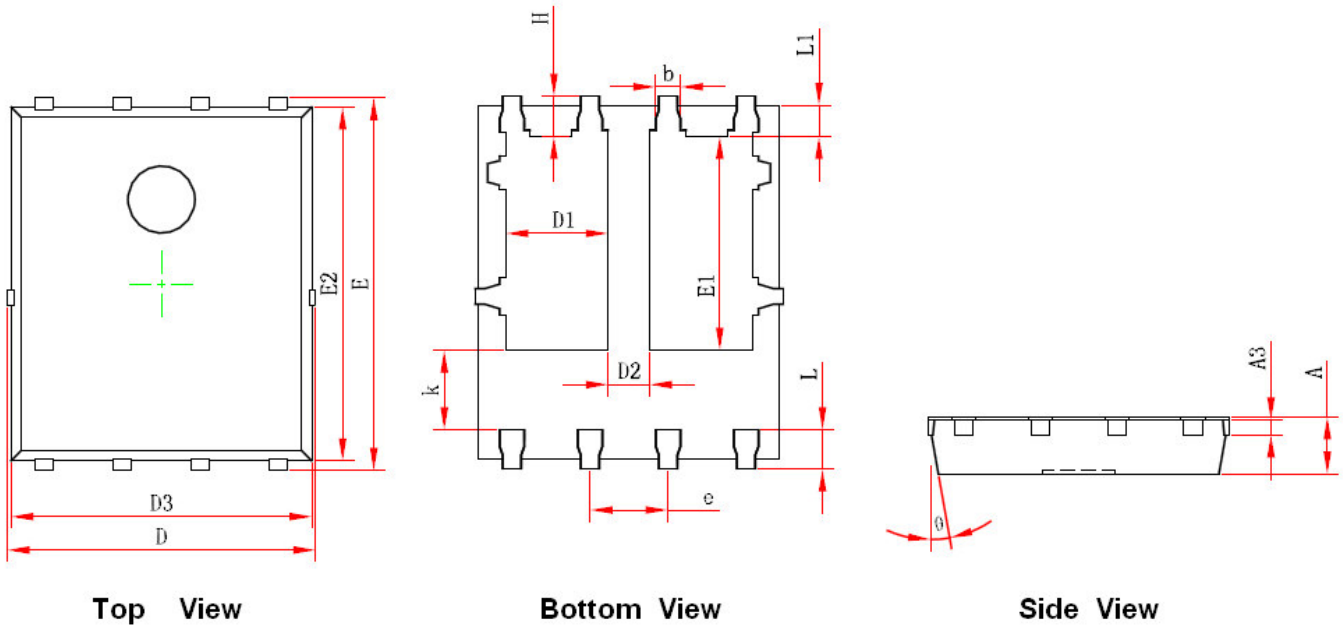


Unclamped Inductive Switching Test Circuit & Waveforms





Package Information (DFN 5X6-8L)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254 REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	1.470	1.870	0.058	0.074
D2	0.470	0.870	0.019	0.034
E1	3.375	3.575	0.133	0.141
D3	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

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