



## General Description

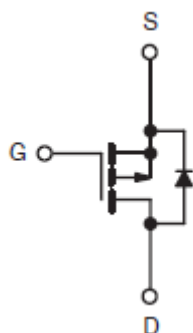
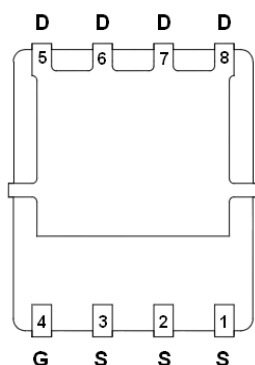
AFP7489S, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent  $R_{DS(ON)}$ , low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

## Features

- $I_D = -7.8A, R_{DS(ON)} = 42m\Omega @ V_{GS} = -10V$
- $I_D = -7.3A, R_{DS(ON)} = 47m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- DFN5X6-8L package design

## Pin Description ( DFN5X6-8L )



## Application

- Load Switch
- Adaptor Switch
- Notebook PC

## Pin Define

Pin	Symbol	Description
4	G	Gate
1~3	S	Source
5~8	D	Drain

## Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFP7489SFN568RG	7489S	DFN5X6-8L	Tape & Reel	2500 EA

- ※ 7489S : Parts Code
- ※ YYMMDD : Date code
- ※ AFP7489SFN568RG : 13" Tape & Reel ; Pb- Free ; Halogen- Free



**Absolute Maximum Ratings**

( $T_A=25^{\circ}\text{C}$  Unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-100	V
Gate –Source Voltage	$V_{GSS}$	$\pm 20$	V
Continuous Drain Current( $T_J=150^{\circ}\text{C}$ )	$I_{DSM}$	$T_A=25^{\circ}\text{C}$	-7.8
		$T_A=70^{\circ}\text{C}$	-6.2
Pulsed Drain Current	$I_{DM}$	-40	A
Continuous Source Current(Diode Conduction)	$I_S$	-4.3	
Single Pulse Avalanche Current	$I_{AS}$	-35	
Power Dissipation	$P_{DSM}$	$T_A=25^{\circ}\text{C}$	5.2
		$T_A=75^{\circ}\text{C}$	3.3
Operating Junction Temperature	$T_J$	150	$^{\circ}\text{C}$
Storage Temperature Range	$T_{STG}$	-55/150	$^{\circ}\text{C}$
Thermal Resistance-Junction to Ambient	$t \leq 10 \text{ s}$	$R_{\theta JA}$	19
Thermal Resistance-Junction to Case	Steady-State	$R_{\theta JC}$	1.2

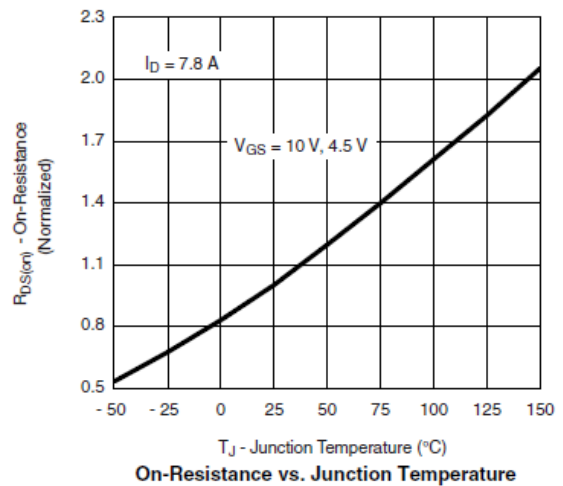
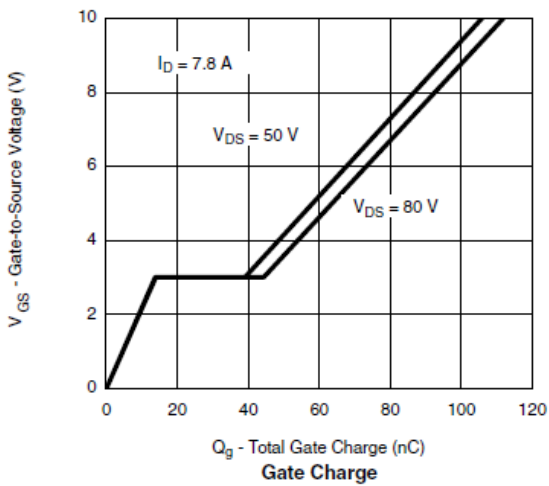
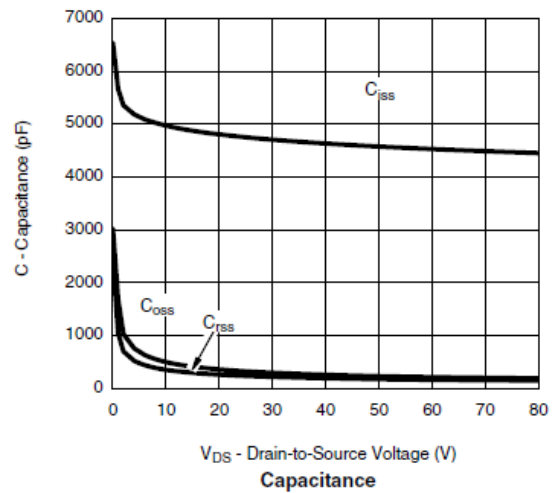
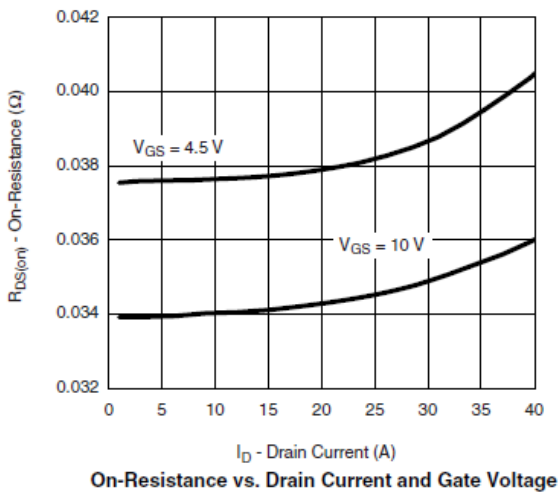
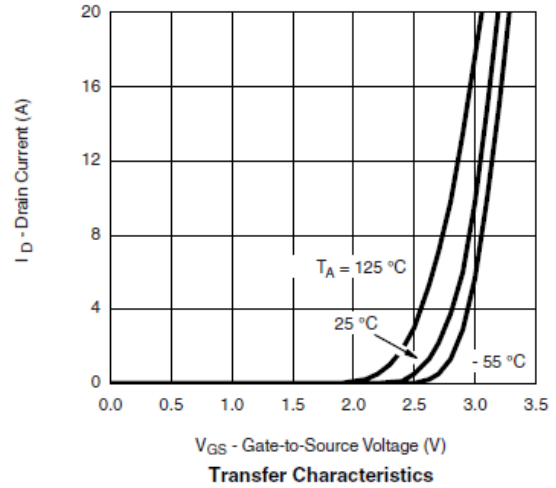
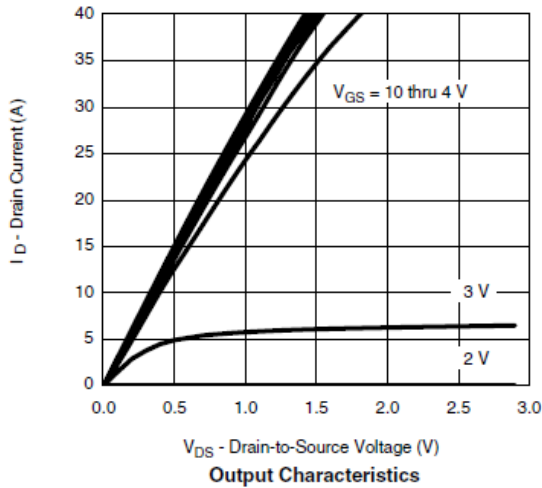
**Electrical Characteristics**

( $T_A=25^{\circ}\text{C}$  Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D = -250\mu A$	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D = -250\mu A$	-1.0		-2.5	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS} = \pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -80V, V_{GS}=0V$			-1	uA
		$V_{DS} = -80V, V_{GS}=0V$ $T_J=85^{\circ}\text{C}$			-30	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq -5V, V_{GS} = -10V$	-40			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -7.8A$		38	42	m $\Omega$
		$V_{GS} = -4.5V, I_D = -7.3A$		42	47	
Forward Transconductance	$g_{FS}$	$V_{DS} = -15V, I_D = -7.8A$		38		S
Diode Forward Voltage	$V_{SD}$	$I_S = -2A, V_{GS}=0V$		-0.8	-1.3	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS} = -50V, V_{GS} = -4.5V$ $I_D = -7.8A$		55	100	nC
Gate-Source Charge	$Q_{gs}$			15		
Gate-Drain Charge	$Q_{gd}$			25		
Input Capacitance	$C_{iss}$	$V_{DS} = -50V, V_{GS} = 0V$ $f = 1\text{MHz}$		4600		pF
Output Capacitance	$C_{oss}$			230		
Reverse Transfer Capacitance	$C_{rss}$			175		
Turn-On Time	$t_{d(on)}$	$V_{DD} = -50V, R_L = 8.1\Omega$ $I_D = -6.2A, V_{GEN} = -10V$ $R_G = 1\Omega$		15	30	ns
	$t_r$			20	40	
Turn-Off Time	$t_{d(off)}$			110	180	
	$t_f$			100	170	

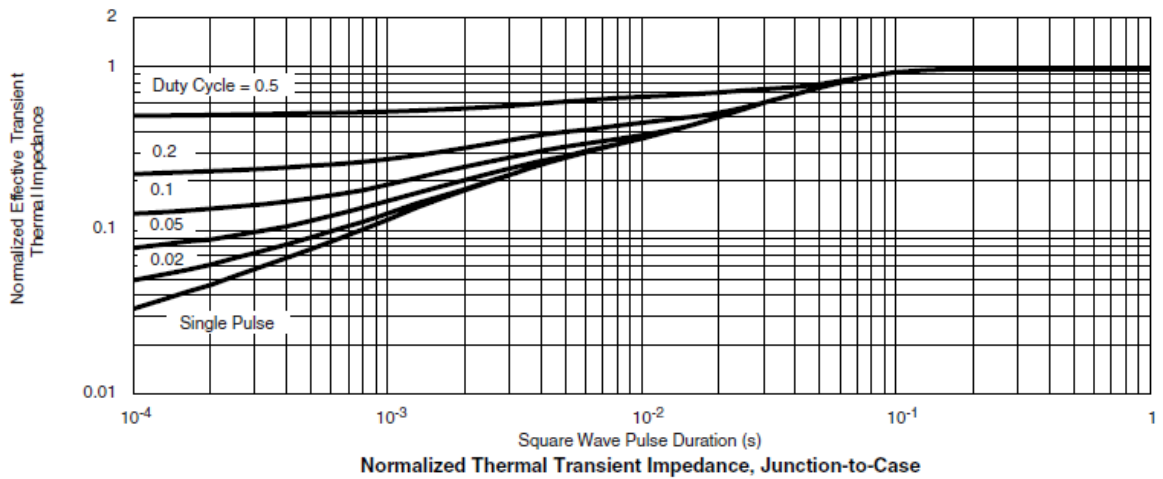
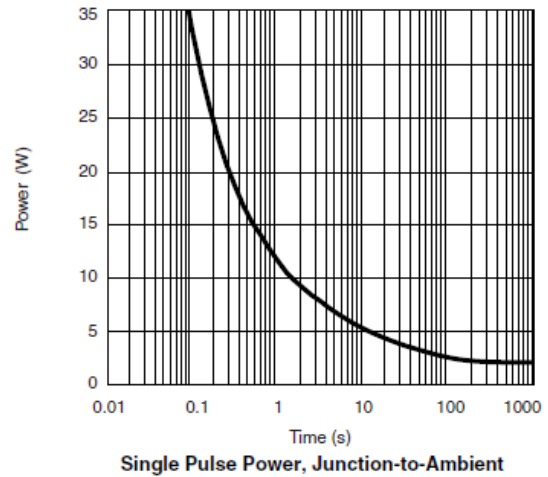
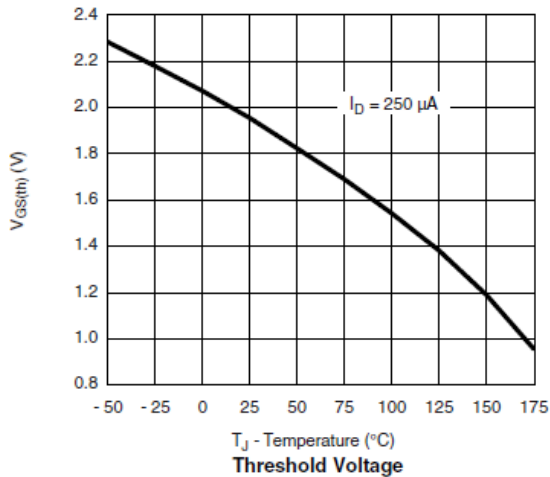
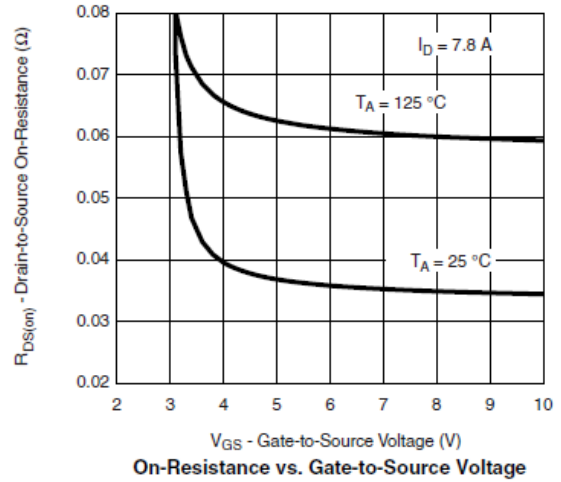
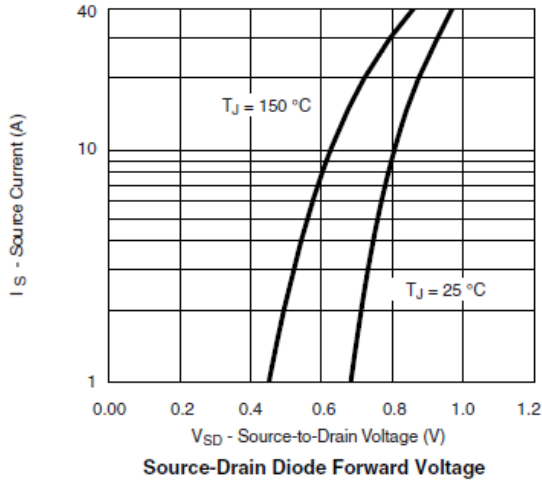


## Typical Characteristics





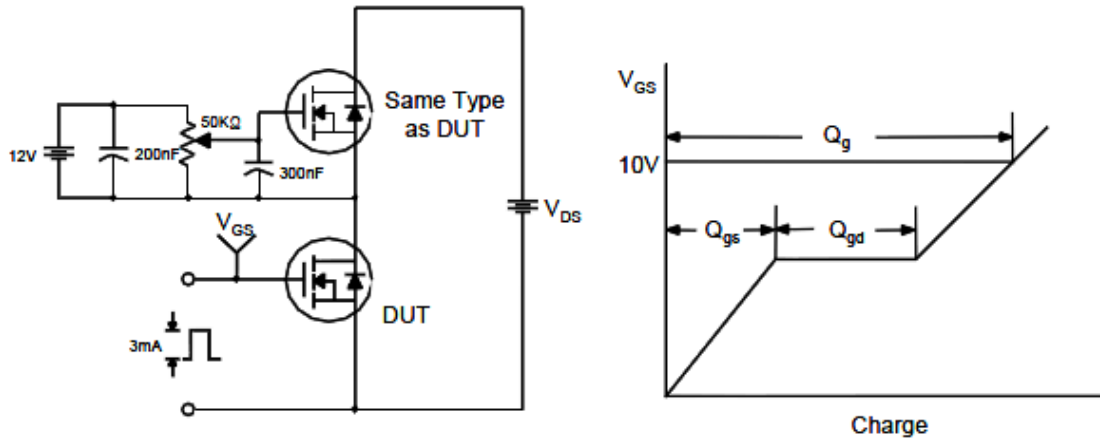
## Typical Characteristics



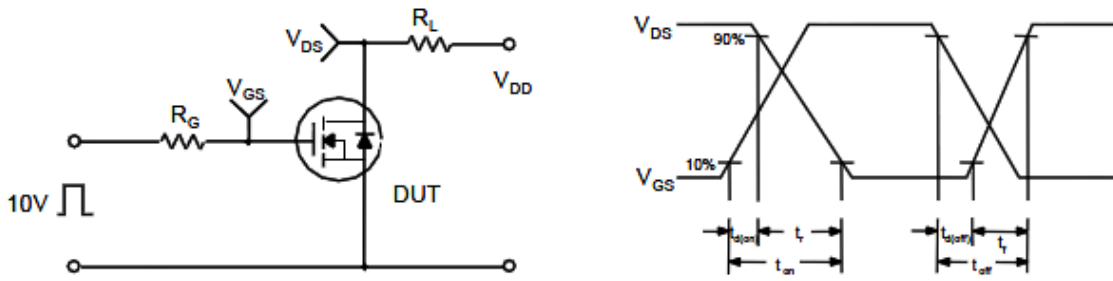


**Typical Characteristics**

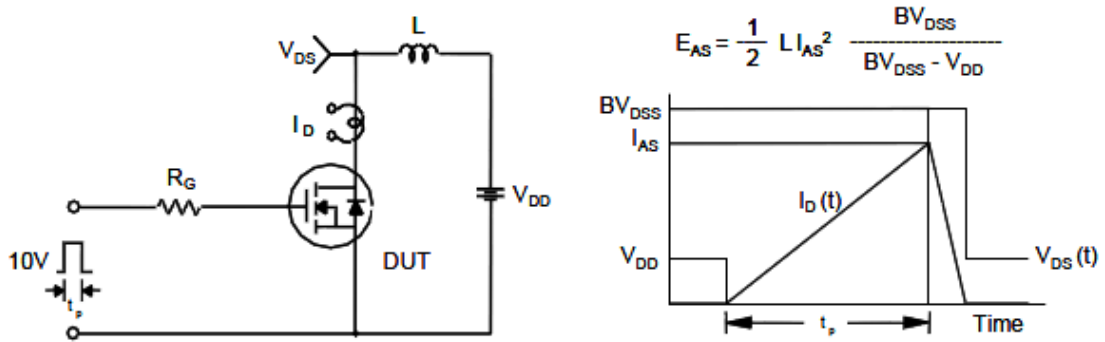
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

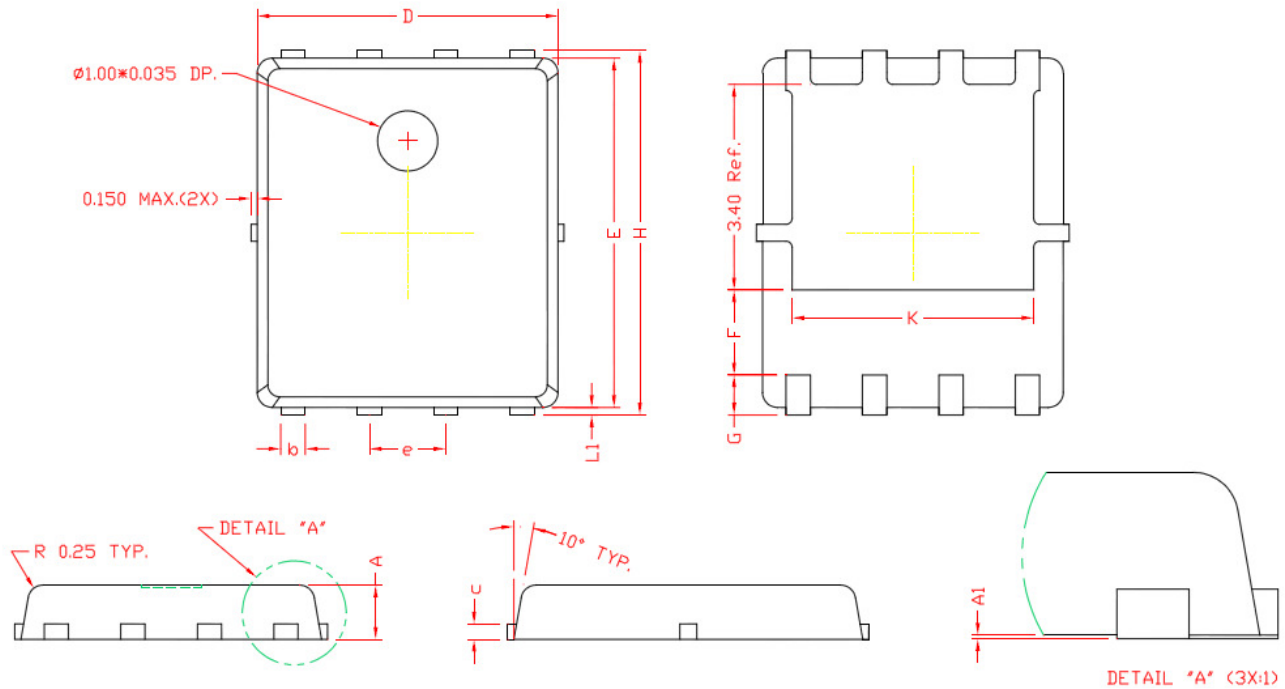


Unclamped Inductive Switching Test Circuit & Waveforms





**Package Information ( DFN5X6-8L )**



**DIMENSIONS**

REF.	Millimeters		REF.	Millimeters	
	Min.	Max.		Min.	Max.
A	0.80	1.00	E	5.70	5.90
A1	0.00	0.05	e	1.27 BSC.	
b	0.35	0.49	H	5.95	6.20
c	0.254 Ref.		L1	0.10	0.18
D	4.90	5.10	G	0.60 Ref.	
F	1.40 Ref.		K	4.00 Ref.	

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